PRELIMINARY

Élan™ Am386® SC300

Highly Integrated, Low-Power, 32-Bit Microprocessor and System Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Highly Integrated Single Chip CPU and System Logic**
  - Optimized for handheld systems
  - Combines 32-bit, x86 compatible, low-voltage CPU with memory controller, PC/AT peripheral controllers, real-time clock, and PLL clock generators
  - 0.7-micron, 2-layer metal, low-voltage, CMOS process fully static
- **Enhanced Am386® SXLV CPU Core**
  - 25-MHz or 33-MHz operating frequencies
  - 3.3-V core, 3.3-V or 5-V memory and I/O
  - Low-power fully static design for long battery life
  - System Management Mode (SMM) for power management control
- **Integrated Power Management Functions**
  - Internal clock generators (using multiple phase locked loops and one external 32-kHz crystal)
  - Supports CPU System Management Mode (SMM)
  - Multiple operating modes: High Speed PLL, Low Speed PLL, Doze, Sleep, Suspend, and Off. Fully static design allows stopped clock.
  - Comprehensive control of system and peripheral clocks
  - Five external management control pins
  - Suspend refresh of DRAM array
  - Clock switching during ISA cycles
  - Low power consumption: 0.12 mW typical Suspend mode power
  - Simultaneous multiple-voltage I/O pads operate at either 3.3 V or 5 V. Core operates at 3.3 V for minimum power consumption.
- **Integrated Memory Controller**
  - Controls symmetrically addressable DRAM or asymmetrical 512Kbyte x 8-bit or 1Mbyte x 16-bit DRAM or SRAM as main memory
  - Zero wait-state access with 70-ns, Page Mode DRAMs
  - Supports up to 16-Mbyte system memory
  - Supports up to 16 Mbytes of application ROM/ Flash, and 320-Kbyte direct ROM BIOS access. Also supports shadow RAM
  - Fully PC/AT compatible
- **Integrated PC/AT Compatible Peripheral Logic**
  - One programmable interval timer (fully 8254 compatible)
  - Two programmable interrupt controllers (8259A compatible)
  - Two DMA controllers (8237A compatible)
  - Built-in Real Time Clock (146818A compatible), with an additional 114 bytes of RAM
  - Internal Phase Locked Loops (PLL) generate all clocks from single 32.768-kHz crystal input
- **Bus Configurations**
  - 16-bit data path
  - Optional bus configurations:
    - Internal LCD controller with sub ISA
    - 386 local bus with sub ISA
    - Maximum ISA Bus mode
  - Four programmable chip selects
  - Built-in 8042 chip select
- **Serial Port Controller (16450 UART Compatible)**
- **Bidirectional Parallel Port with EPP**
- **Integrates Two PCMCIA Version 2.1 Slot Controllers**
- **Integrated CGA-Compatible LCD Controller**
  - Fully 6845 compatible
  - 16 gray levels in Text mode; 2 or 4 levels in Graphics mode
  - Supports the following LCD Panel Sizes:
    - 320 x 200 single scan (2 bit)
    - 640 x 200 single/dual scan (1 bit)
    - 480 x 320 single scan (1 bit)

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GENERAL DESCRIPTION

The Élan™ Am386®SC300 device is a highly integrated, low-voltage, single-chip implementation of the Am386SXLV microprocessor plus most of the additional logic needed for an AT-compatible personal computer. It is ideal for palm-top computers and Personal Digital Assistants (PDAs). It combines an Am386SXLV low-voltage microprocessor core with a memory control unit, a power management unit (PMU), and the standard system, ISA bus, and peripheral control logic of a PC/AT-compatible computer. In addition, the chip includes a 146818A-compatible real-time clock, internal phase locked loops for clock generation, and a local bus controller.

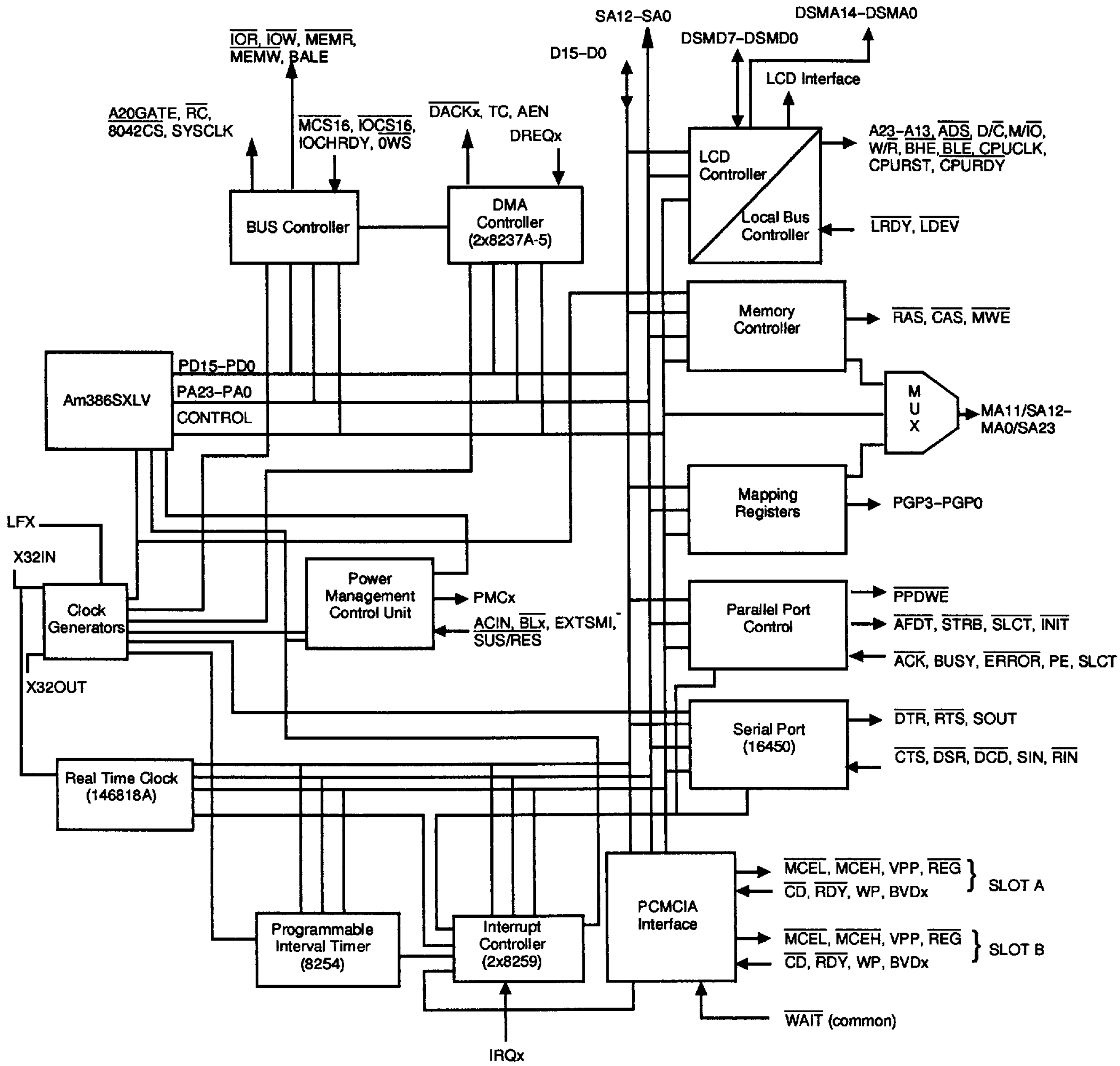
The Am386SC300 microprocessor from AMD® is the first in a family of mobile computing products from the Embedded Processor Division (EPD). EPD provides standard products for the handheld, palm-top, and PDA computer markets, leveraging AMD core modules. The Am386SC300 microprocessor demonstrates the feasibility of constructing highly integrated components built from standard cores and getting these products to market quickly.

The Am386SC300 microprocessor has integrated all the system and peripheral control logic of a chipset for a portable computer, plus built-in 16450 UART, two PCMCIA Version 2.1 slots, power management functions, memory controller, bus controller, standard PC logic chips (8259A, 8237A, and 8254), and a built-in CGA-compatible LCD controller.

The Élan device's true static design and low operating voltage enable longer battery life and lower weight for handheld applications. The internal core of the Am386SC300 microprocessor operates at 3.3 V, and the I/O pads allow either 3.3-V or 5-V operation. Lowering typical operating voltage from 5 V to 3.3 V can dramatically increase battery life.

Functionally, the Élan device is a PC/AT-compatible computer on a chip that is designed to furnish the customer with a high-performance, low-power system solution, providing state-of-the-art power management in a small physical footprint. The Élan Am386SC300 microprocessor is available in both 208-pin Plastic Quad Flat Pack (PQFP) and Thin Quad Flat Pack (TQFP) packages.

BLOCK DIAGRAM



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ORDERING INFORMATION

AMD standard products are available in several packages and operating ranges. The order numbers (Valid Combinations) are formed by a combination of the elements below.

Am386SC300 -25 K C \W

OPTIONAL PROCESSING
\W =Trimmed and formed

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)

PACKAGE TYPE
K = 208-pin PQFP (Plastic Quad Flat Pack)
V = 208-pin TQFP (Thin Quad Flat Pack)

SPEED OPTION
-33 = 33 MHz
-25 = 25 MHz

DEVICE NUMBER/DESCRIPTION
Am386SC300 highly integrated, low-power, 32-bit microprocessor and system logic

Valid Combinations	
Am386SC300-25	KC\W
Am386SC300-33	KC\W
Am386SC300-25	VC\W
Am386SC300-33	VC\W

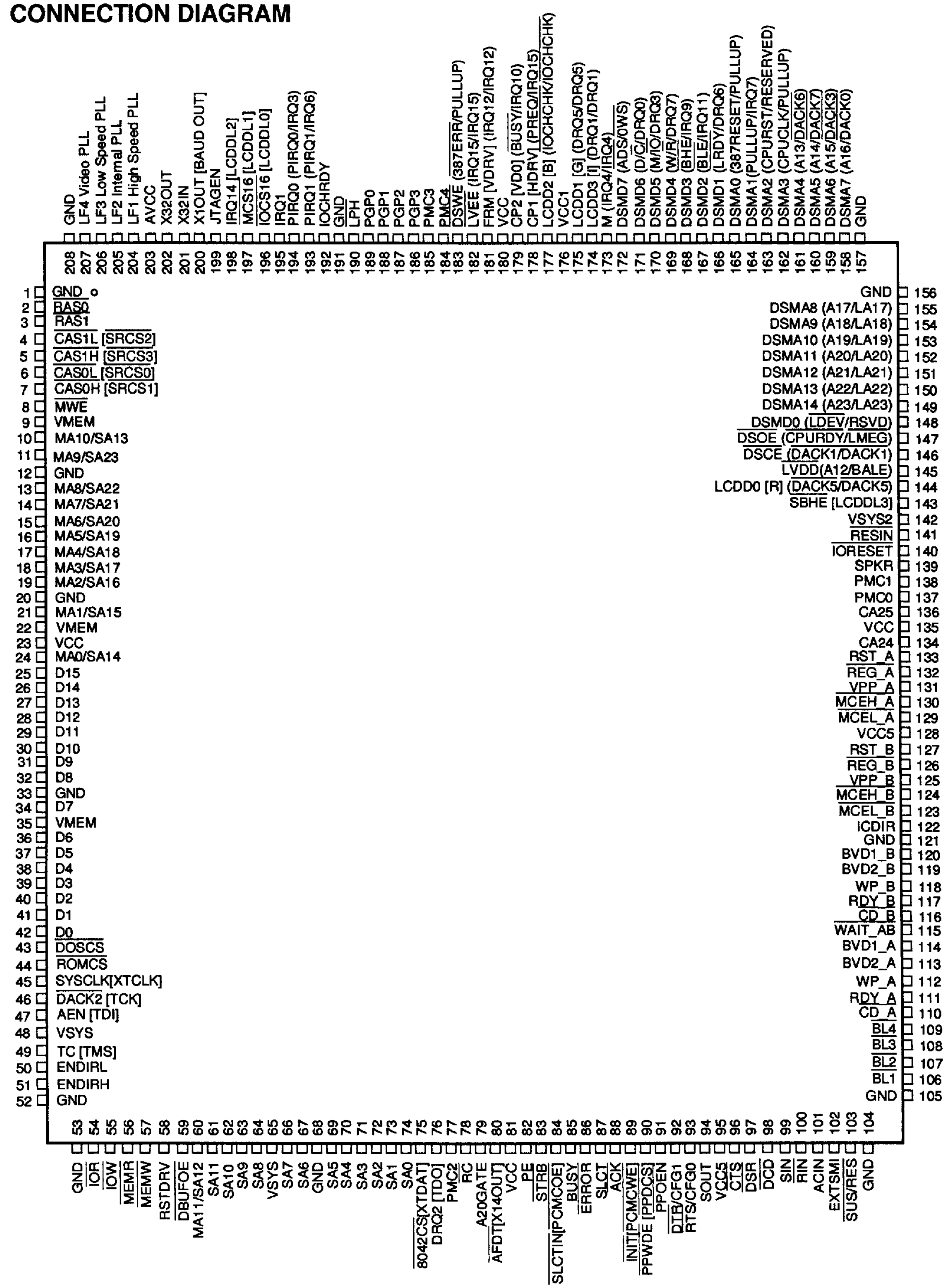
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

TABLE OF CONTENTS

ÉLAN Am386SC300 MICROPROCESSOR

CONNECTION DIAGRAM



Note: *Pin 1 is marked for designation purposes only.*

Am386SC300 Pin Designations

This section, beginning with the Connection Diagram on the preceding page, identifies the pins of the Élan device and lists the signals associated with each pin. Tables 1–10 of the Pin Characteristics section group these signals according to function.

The Signal Name column in the pin designation table that follows, and in Tables 1–10, is decoded as follows:

NAME1 / NAME2 [NAME3] (NAME4 / NAME5)

NAME1 - This is the pin function when the Élan Am386SC300 device has been configured, at reset, for the internal LCD Controller mode of operation. If the pin only has one function regardless of the mode, NAME1 is the only name given.

NAME2 - This is the secondary pin function (by default) when the Élan device has been configured, at reset, for the internal LCD Controller mode of operation. If the pin always has two functions regardless of the mode, NAME1 followed by NAME2 are the only names given.

NAME3 - This is a tertiary pin function that must be enabled specificalkly by firmware. As an example, for pins DACK2[TCK], DRQ2[TDO], AEN[TDI], and TC[TMS], the NAME3 function is selected by the JTAGEN pin being asserted High (JTAG ENABLE).

NAME4 - Designates the pin function when the Élan device has been configured, at reset, for the Local Bus mode of operation.

NAME5 - Designates the pin function when the Élan device has been configured, at reset, for the Maximum ISA mode of operation.

PIN DESIGNATIONS (Sorted by Pin Number)

Pin No.	Signal Name (Alternate Functions)	Pin No.	Signal Name (Alternate Functions)	Pin No.	Signal Name (Alternate Functions)
1	GND	31	D9	61	SA11
2	$\overline{RAS0}$	32	D8	62	SA10
3	$\overline{RAS1}$	33	GND	63	SA9
4	$\overline{CAS1L}$ [$\overline{SRCS2}$]	34	D7	64	SA8
5	$\overline{CAS1H}$ [$\overline{SRCS3}$]	35	VMEM	65	VSYS
6	$\overline{CAS0L}$ [$\overline{SRCS0}$]	36	D6	66	SA7
7	$\overline{CAS0H}$ [$\overline{SRCS1}$]	37	D5	67	SA6
8	$\overline{MWE}$	38	D4	68	GND
9	VMEM	39	D3	69	SA5
10	MA10/SA13	40	D2	70	SA4
11	MA9/SA23	41	D1	71	SA3
12	GND	42	D0	72	SA2
13	MA8/SA22	43	$\overline{DOSCS}$	73	SA1
14	MA7/SA21	44	$\overline{ROMCS}$	74	SA0
15	MA6/SA20	45	SYSCLK [XTCLK]	75	$\overline{8042CS}$ [XTDAT]
16	MA5/SA19	46	$\overline{DACK2}$ [TCK]	76	DRQ2 [TDO]
17	MA4/SA18	47	AEN [TDI]	77	PMC2
18	MA3/SA17	48	VSYS	78	RC
19	MA2/SA16	49	TC [TMS]	79	A20GATE
20	GND	50	ENDIRL	80	$\overline{AFDT}$ [X14OUT]
21	MA1/SA15	51	ENDIRH	81	VCC
22	VMEM	52	GND	82	PE
23	VCC	53	GND	83	$\overline{STRB}$
24	MA0/SA14	54	$\overline{IOR}$	84	$\overline{SLCTIN}$ [PCMCOE]
25	D15	55	$\overline{IOW}$	85	BUSY
26	D14	56	$\overline{MEMR}$	86	$\overline{ERROR}$
27	D13	57	$\overline{MEMW}$	87	SLCT
28	D12	58	RSTDRV	88	$\overline{ACK}$
29	D11	59	$\overline{DBUFOE}$	89	$\overline{INIT}$ [$\overline{PCMCWE}$]
30	D10	60	MA11/SA12	90	$\overline{PPDWE}$ [$\overline{PPDCS}$]

PIN DESIGNATIONS (Sorted by Pin Number), continued

Pin No.	Signal Name (Alternate Functions)	Pin No.	Signal Name (Alternate Functions)	Pin No.	Signal Name (Alternate Functions)
91	PPOEN	119	BVD2_B	147	DSOE (CPURDY/LMEG)
92	DTR/CFG1	120	BVD1_B	148	DSMD0 (LDEV/RSVD)
93	RTS/CFG0	121	GND	149	DSMA14 (A23/LA23)
94	SOUT	122	ICDIR	150	DSMA13 (A22/LA22)
95	VCC5	123	MCEL_B	151	DSMA12 (A21/LA21)
96	CTS	124	MCEH_B	152	DSMA11 (A20/LA20)
97	DSR	125	VPP_B	153	DSMA10 (A19/LA19)
98	DCD	126	REG_B	154	DSMA9 (A18/LA18)
99	SIN	127	RST_B	155	DSMA8 (A17/LA17)
100	RIN	128	VCC5	156	GND
101	ACIN	129	MCEL_A	157	GND
102	EXTSMI	130	MCEH_A	158	DSMA7 (A16/DACK0)
103	SUS/RES	131	VPP_A	159	DSMA6 (A15/DACK3)
104	GND	132	REG_A	160	DSMA5 (A14/DACK7)
105	GND	133	RST_A	161	DSMA4 (A13/DACK6)
106	BL1	134	CA24	162	DSMA3 (CPUCLK/PULLUP)
107	BL2	135	VCC	163	DSMA2 (CPURST/RSVD)
108	BL3	136	CA25	164	DSMA1 (PULLUP/IRQ7)
109	BL4	137	PMC0	165	DSMA0 (387RESET/ PULLUP)
110	CD_A	138	PMC1	166	DSMD1 (LRDY/DRQ6)
111	RDY_A	139	SPKR	167	DSMD2 (BLE/IRQ11)
112	WP_A	140	IORESET	168	DSMD3 (BHE/IRQ9)
113	BVD2_A	141	RESIN	169	DSMD4 (W/R/DRQ7)
114	BVD1_A	142	VSYS2	170	DSMD5 (M/IO/DRQ3)
115	WAIT_AB	143	SBHE [LCDDL3]	171	DSMD6 (D/C/DRQ0)
116	CD_B	144	LCDD0 [R](DACK5/ DACK5)	172	DSMD7 (ADS/0WS)
117	RDY_B	145	LVDD (A12/BALE)	173	M (IRQ4/IRQ4)
118	WP_B	146	DSCE (DACK1/ DACK1)	174	LCDD3 [I] (DRQ1/DRQ1)

PIN DESIGNATIONS (Sorted by Pin Number), continued

Pin No.	Signal Name (Alternate Functions)	Pin No.	Signal Name (Alternate Functions)	Pin No.	Signal Name (Alternate Functions)
175	LCDD1 [G] (DRQ5/DRQ5)	186	PGP3	197	$\overline{\text{MCS16}}$ [LCDDL1]
176	VCC1	187	PGP2	198	IRQ14 [LCDDL2]
177	LCDD2 [B] ($\overline{\text{IOCHCHK}}$/ IOCHCHK)	188	PGP1	199	JTAGEN
178	CP1 [HDRV] (PREQ/IRQ5)	189	PGP0	200	X1OUT [BAUD_OUT]
179	CP2 [VD0] ($\overline{\text{BUSY}}$/IRQ10)	190	$\overline{\text{LPH}}$	201	X32IN
180	VCC	191	GND	202	X32OUT
181	FRM [VDRV] (IRQ12/ IRQ12)	192	IOCHRDY	203	AVCC
182	$\overline{\text{LVEE}}$ (IRQ15/IRQ15)	193	PIRQ1 (PIRQ1/IRQ6)	204	LF1
183	$\overline{\text{DSWE}}$ ($\overline{\text{387ERR}}$/PULLUP)	194	PIRQ0 (PIRQ0/IRQ3)	205	LF2
184	PMC4	195	IRQ1	206	LF3
185	PMC3	196	$\overline{\text{IOCS16}}$ [LCDDL0]	207	LF4
				208	GND

PIN CHARACTERISTICS

To clarify the meaning of the column headings of Tables 1 through 10, the Pin Characteristics tables:

The letters in the **I/O Type** column of Tables 1-10 mean the following:

I - Input

O - Output

STI - Schmitt Trigger Input

B- - Bidirectional

A- - Analog

The **Term** column refers to internal termination. The letters in this column of Tables 1–10 mean the following:

PD - Pull Down Resistor

PU - Pull Up Resistor

The symbols (letters) in the **Drive Type** column specify the drive capability of output pins. These specifications can be found in the DC Characteristics section of this document. For a more complete description of I/O Drive Types, see Table 34 on page 74.

The **Clock Off** column describes the logic level of the I/O pins while the Am386SC300 device is in any of the power management modes where the CPU clock is stopped. For Doze mode, the data reflects a situation in which the internal CGA controller video refresh is disabled.

The **Reset State** column lists the I/O pin voltage level when all of the VCC pins are stable and the $\overline{\text{RESIN}}$ input is active. The level of the VCC pins correlating to this data is as follows:

	Internal CGA (V)	Local Bus (V)	Maximum ISA (V)
VCC	3.3	3.3	3.3
AVCC	3.3	3.3	3.3
VCC5	5.0	5.0	5.0
VSYS2	3.3	3.3	5.0
VSYS	5.0	5.0	5.0
VMEM	3.3	3.3	3.3
VCC1	3.3	3.3	3.3

The **VCCIO** column refers to the voltage supply pin on the Am386SC300 microprocessor that is directly connected to the output driver for the specified signal pin.

The **VCC Clamp** column refers to the voltage supply pin on the Am386SC300 microprocessor that is directly connected to the ESD protection diode (cathode) for the specified signal pin. Any pin with a 5-V VCC Clamp is a "5-V safe" input.

The **Spec. Load** (specification load) column is used to determine derated AC timing. See the Derating Curves section of this data sheet.

Table 1. Memory Bus Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
$\overline{\text{RAS0}}$ [1,3]	2	O		E,D,C	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	50
$\overline{\text{RAS1}}$ [1,3]	3	O		E,D,C	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	50
$\overline{\text{CAS1L}}$ [$\overline{\text{SRCS2}}$] [1,2]	4	O		D	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	30
$\overline{\text{CAS1H}}$ [$\overline{\text{SRCS3}}$] [1,2]	5	O		D	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	30
$\overline{\text{CAS0L}}$ [$\overline{\text{SRCS0}}$] [1,2]	6	O		D	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	30
$\overline{\text{CAS0H}}$ [$\overline{\text{SRCS1}}$] [1,2]	7	O		D	Active	3.3/0	3.3/0	3.3/0	VMEM	VMEM	30
MA10/SA13 [3]	10	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA9/SA23 [3]	11	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA8/SA22 [3]	13	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA7/SA21 [3]	14	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA6/SA20 [3]	15	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA5/SA19 [3]	16	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA4/SA18 [3]	17	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA3/SA17 [3]	18	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA2/SA16 [3]	19	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA1/SA15 [3]	21	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
MA0/SA14 [3]	24	O		E,D,C	0	3.3	3.3	3.3	VMEM	VMEM	70
$\overline{\text{MWE}}$ [3]	8	O		E,D,C	1	3.3	3.3	3.3	VMEM	VMEM	70
$\overline{\text{ROMCS}}$	44	O		B	1	5.0	5.0	5.0	VSYS	VCC5	30
$\overline{\text{DOSCS}}$	43	O		B	1	5.0	5.0	5.0	VSYS	VCC5	50

Notes:

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

1. *These signals are active during reset.*
2. *These pins always default to their DRAM interface function.*
3. *The drive strength for these pins is programmable. E is the default.*

Table 2. System Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
MA11/SA12	60	O		E	0	5.0	5.0	5.0	VSYS	VCC5	70
SA11	61	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA10	62	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA9	63	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA8	64	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA7	66	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA6	67	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA5	69	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA4	70	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA3	71	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA2	72	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA1	73	O		D	0	5.0	5.0	5.0	VSYS	VCC5	70
SA0	74	O		D	0	0.0	0.0	0.0	VSYS	VCC5	70
D15 (2)	25	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D14(2)	26	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D13(2)	27	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D12(2)	28	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D11(2)	29	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D10(2)	30	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D9(2)	31	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D8(2)	32	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D7(2)	34	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D6(2)	36	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D5(2)	37	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70

Table 2. System Interface (continued)

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
D4[2]	38	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D3[2]	39	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D2[2]	40	B	PD	E,D,C	0	0.0	0.0	0.0	VMEM	VMEM	70
D1[2]	41	B	PD	E,D,C	0	0.0	3.3	0.0	VMEM	VMEM	70
D0[2]	42	B	PD	E,D,C	0	0.0	3.3	0.0	VMEM	VMEM	70
SYSCLK[XTCLK][1]	45	O(STI)		B	0(–)	5.0/0	5.0/0	5.0/0	VSYS	VCC5	30
IRQ1	195	I	PU	–	–	4.4	4.4	4.4	VCC1	VCC5	
PIRQ1(PIRQ1/ IRQ6)	193	I	PU	–(–/–)	–(–/–)	3.3	3.3	3.3	VCC1	VCC5	
PIRQ0(PIRQ0/ IRQ3)	194	I	PU	–(–/–)	–(–/–)	3.3	3.3	3.3	VCC1	VCC5	
$\overline{\text{DACK2}}$ [TCK]	46	O(I)		B	1	5.0	5.0	5.0	VSYS	VCC5	30
DRQ2 [TDO]	76	I(O)	PD	A	–	0.0	0.0	0.0	VSYS	VCC5	30
AEN [TDI]	47	O(I)		B	1	0.0	0.0	0.0	VSYS	VCC5	30
TC [TMS]	49	O(I)		B	0	0.0	0.0	0.0	VSYS	VCC5	30
ENDIRL	50	O		B	1	5.0	5.0	5.0	VSYS	VCC5	30
ENDIRH	51	O		B	1	5.0	5.0	5.0	VSYS	VCC5	30
$\overline{\text{DBUFOE}}$	59	O		B	1	5.0	5.0	5.0	VSYS	VCC5	30
$\overline{\text{IOR}}$	54	O		C	1	5.0	5.0	5.0	VSYS	VCC5	50
$\overline{\text{IOW}}$	55	O		C	1	5.0	5.0	5.0	VSYS	VCC5	50
$\overline{\text{MEMR}}$	56	O		C	1	5.0	5.0	5.0	VSYS	VCC5	50
$\overline{\text{MEMW}}$	57	O		C	1	5.0	5.0	5.0	VSYS	VCC5	50
RSTDRV	58	O		A	0	5.0	5.0	5.0	VSYS	VCC5	30
IOCHRDY	192	STI	PU	–	–	3.3	3.3	3.3	VCC1	VCC5	

Notes:

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

1. *Reset State SYSCLK frequency is 4.6 MHz.*
2. *The drive strength for these pins is programmable. E is the default.*

Table 3. Keyboard Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
$\overline{\text{8042CS}}$ [XTDAT]	75	O(STI)		B	1(–)	5.0	5.0	5.0	VSYS	VCC5	30
$\overline{\text{RC}}$	78	I	PU	–	–	5.0	5.0	5.0	VSYS	VCC5	
A20GATE	79	I	PU	–	–	5.0	5.0	5.0	VSYS	VCC5	

Note:
All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

Table 4. Parallel Port Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
$\overline{\text{AFDT}}$ [X14OUT] (1)	80	O		D	Last state	5.0	5.0	5.0	VCC5	VCC5	100
$\overline{\text{INIT}}$[$\overline{\text{PCMCWE}}$] (1)	89	O		D	Last state	0.0	0.0	0.0	VCC5	VCC5	100
$\overline{\text{STRB}}$ (1)	83	O		D	Last state	5.0	5.0	5.0	VCC5	VCC5	100
$\overline{\text{SLCTIN}}$ [$\overline{\text{PCMCOE}}$] (1)	84	O		D	Last state	5.0	5.0	5.0	VCC5	VCC5	100
$\overline{\text{ACK}}$	88	I		–	–	5.0	5.0	5.0	VCC5	VCC5	
BUSY (2)	85	I		–	–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{\text{ERROR}}$	86	I		–	–	5.0	5.0	5.0	VCC5	VCC5	
PE	82	I		–	–	5.0	5.0	5.0	VCC5	VCC5	
SLCT	87	I		–	–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{\text{PPDWE}}$ [$\overline{\text{PPDCS}}$]	90	O		B	1(1)	5.0	5.0	5.0	VCC5	VCC5	30
$\overline{\text{PPOEN}}$	91	O		B	1(1)	0.0	0.0	0.0	VCC5	VCC5	30

Notes:
All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

1. *These outputs function as open-drain outputs in Normal Parallel Port mode, and function as CMOS drivers when the EPPEN configuration bit is set.*
2. *The parallel port interface BUSY input must have an external pull-up if the parallel port is to be used in EPP mode. If this pull-up is not present, accesses to the parallel port in EPP mode will lock up the system.*

Table 5. Serial Port Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
$\overline{DTR}$/CFG1(1)	92	O		A	Last state	0.0	5.0	0	VCC5	VCC5	50
$\overline{RTS}$/CFG0(1)	93	O		A	Last state	0.0	0.0	5.0	VCC5	VCC5	50
SOUT	94	O		A	Last state	0.0	0.0	5.0	VCC5	VCC5	50
$\overline{CTS}$	96	I	PU		-	5.0	5.0	5.0	VCC5	VCC5	
$\overline{DCD}$	98	I	PU		-	5.0	5.0	5.0	VCC5	VCC5	
$\overline{DSR}$	97	I	PU		-	5.0	5.0	5.0	VCC5	VCC5	
$\overline{RIN}$	100	I	PU		-	5.0	5.0	5.0	VCC5	VCC5	
SIN	99	I	PU		-	5.0	5.0	5.0	VCC5	VCC5	

Notes:

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

1. *These pins are terminated externally per bus option selection.*

Table 6. Power Management Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
ACIN	101	STI	PD	–	–	0.0	0.0	0.0	VCC5	VCC5	
EXTSMI	102	STI	PD	–	–	0.0	0.0	0.0	VCC5	VCC5	
$\overline{\text{SUS}}$/RES	103	STI		–	–	5.0	5.0	5.0	VCC5	VCC5	
PMC4 (1)	184	O		B	Active	0.0	0.0	0.0	VCC1	VCC5	50
PMC3 (1)	185	O		B	Active	3.3	3.3	3.3	VCC1	VCC5	50
PMC2 (1)	77	O		B	Active	0.0	0.0	0.0	VSYS	VCC5	50
PMC1 (1)	138	O		B	Active	0.0	0.0	0.0	VCC5	VCC5	50
PMC0 (1)	137	O		B	Active	0.0	0.0	0.0	VCC5	VCC5	50
PGP3	186	O		B	Active	3.3	3.3	3.3	VCC5	VCC1	50
PGP2	187	O		B	Active	3.3	3.3	3.3	VCC5	VCC1	50
PGP1	188	B		B	Active	3.3	3.3	3.3	VCC5	VCC1	50
PGP0	189	B		B	Active	0.0	0.0	0.0	VCC5	VCC1	50
$\overline{\text{BL1}}$	106	STI		–	–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{\text{BL2}}$	107	STI		–	–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{\text{BL3}}$	108	STI		–	–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{\text{BL4}}$	109	STI		–	–	5.0	5.0	5.0	VCC5	VCC5	
$\overline{\text{LPH}}$	190	O		B	Active	0.0	0.0	0.0	VCC1	VCC5	50

Notes:

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

1. *PMC outputs: four Low (PMC0, PMC1, PMC2, PMC4), one High (PMC3), default state after reset. All five are programmable as either active High or Low after reset.*

Table 7. PCMCIA Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
MCEL_A	129	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
MCEH_A	130	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
VPP_A	131	O		B	Active	0.0	0.0	0.0	VCC5	VCC5	50
REG_A	132	O		B	0	5.0	5.0	5.0	VCC5	VCC5	50
RST_A (1)	133	O		B	3 state	0.0	0.0	0.0	VCC5	VCC5	50
CD_A	110	STI		–	–	5.0	5.0	5.0	VCC5	VCC5	
RDY_A (2)	111	I		–	–	0.0	0.0	0.0	VCC5	VCC5	
WP_A (2)	112	I		–	–	0.0	0.0	0.0	VCC5	VCC5	
BVD2_A (2)	113	STI		–	–	0.0	0.0	0.0	VCC5	VCC5	
BVD1_A (2)	114	STI		–	–	0.0	0.0	0.0	VCC5	VCC5	
WAIT_AB (2)	115	I		–	–	5.0	5.0	5.0	VCC5	VCC5	
ICDIR	122	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
MCEL_B	123	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
MCEH_B	124	O		C	1	5.0	5.0	5.0	VCC5	VCC5	50
VPP_B	125	O		A	Active	0.0	0.0	0.0	VCC5	VCC5	50
REG_B	126	O		A	0	5.0	5.0	5.0	VCC5	VCC5	50
RST_B (1)	127	O		B	3 state	0.0	0.0	0.0	VCC5	VCC5	50
CD_B	116	STI		–	–	5.0	5.0	5.0	VCC5	VCC5	
RDY_B (2)	117	I		–	–	0.0	0.0	0.0	VCC5	VCC5	
WP_B (2)	118	I		–	–	0.0	0.0	0.0	VCC5	VCC5	
BVD2_B (2)	119	STI		–	–	0.0	0.0	0.0	VCC5	VCC5	
BVD1_B (2)	120	STI		–	–	0.0	0.0	0.0	VCC5	VCC5	
CA24	134	O		B	0	0.0	0.0	0.0	VCC5	VCC5	50
CA25	136	O		B	0	0.0	0.0	0.0	VCC5	VCC5	50

Notes:

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

1. *External weak pull-down resistor is required.*
2. *The reset state of these signals will be zero only if the reset state of the PCMCIA power source is zero. All of these pins are required to be pulled up to the PCMCIA power source externally.*

Table 8. Display Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
DSMD7($\overline{\text{ADS}}$/$\overline{\text{0WS}}$)	172	B (O/I)		C	0 (1/–)	0.0	3.3	3.3	VCC1	VCC5	50
DSMD6(D/$\overline{\text{C}}$/ DRQ0) [1]	171	B (O/I)		C	0 (LS/–)	0.0	3.3	0.0	VCC1	VCC5	50
DSMD5(M/$\overline{\text{IO}}$/ DRQ3) [1]	170	B (O/I)		C	0 (LS/–)	0.0	0.0	0.0	VCC1	VCC5	50
DSMD4(W/$\overline{\text{R}}$/ DRQ7) [1]	169	B (O/I)		C	0 (LS/–)	0.0	0.0	0.0	VCC1	VCC5	50
DSMD3($\overline{\text{BHE}}$/ IRQ9) [1]	168	B (O/I)		C	0 (LS/–)	0.0	0.0	3.3	VCC1	VCC5	50
DSMD2($\overline{\text{BLE}}$/ IRQ11) [1]	167	B (O/I)		C	0 (LS/–)	0.0	0.0	3.3	VCC1	VCC5	50
DSMD1($\overline{\text{LRDY}}$/ DRQ6)	166	B (I/I)		C	0 (–/–)	0.0	0.0	0.0	VCC1	VCC5	50
DSMD0($\overline{\text{LDEV}}$/ RSVD)	148	B (I/O)		C	0 (–/3 state)	0.0	3.3	0.0	VSYS2	VCC5	50
DSMA14(A23/ LA23)	149	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA13(A22/ LA22)	150	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA12(A21/ LA21)	151	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA11(A20/ LA20)	152	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA10(A19/ LA19)	153	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA9(A18/LA18)	154	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA8(A17/LA17)	155	O		C	0	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA7(A16/ $\overline{\text{DACK0}}$)	158	O		C	0 (0/1)	3.3	3.3	5.0	VSYS2	VCC5	50

Table 8. Display Interface (continued)

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts) Internal CGA	Reset State (volts) Local Bus	Reset State (volts) Max ISA	VCCIO	VCC Clamp	Spec. Load (pF)
DSMA6(A15/ DACK3)	159	O		C	0 (0/1)	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA5(A14/ DACK7)	160	O		C	0 (0/1)	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA4(A13/ DACK6)	161	O		C	0 (0/1)	3.3	3.3	5.0	VSYS2	VCC5	50
DSMA3(CPUCLK/ PULLUP) (2)	162	O		E	0	3.3	3.3/0	3.3	VCC1	VCC5	50 (30)
DSMA2 (CPURST/ RSVD)	163	O		C	0	3.3	3.3	0.0	VCC1	VCC5	50
DSMA1(PULLUP/ IRQ7)	164	O (I/I)		C	0 (–/–)	3.3	3.3	3.3	VCC1	VCC5	50
DSMA0(387RESET/ PULLUP)	165	O (0/I)		C	0 (0/–)	0.0	3.3	3.3	VCC1	VCC5	50
DSWE (387ERR/ PULLUP)	183	O (I/I)		B	1 (–/–)	3.3	3.3	3.3	VCC1	VCC5	30
DSOE(CPURDY/ LMEG)	147	O		B	1	5.0	0.0	0.0	VSYS2	VCC5	50
DSCE (DACK1/ DACK1)	146	O		B	1	0.0	3.3	5.0	VSYS2	VCC5	30
LCDD3 [I] (DRQ1 / DRQ1)	174	O (I/I)		C	0 (–/–)	0.0	0.0	0.0	VCC1	VCC5	100
LCDD0 [R] (DACK5/ DACK5)	144	O		C	0 (1/1)	3.3	3.3	5.0	VSYS2	VCC5	100
LCDD1 [G] (DRQ5/ DRQ5)	175	O (I/I)		C	0 (–/–)	0.0	3.3	0.0	VCC1	VCC5	100
LCDD2 [B] (IOCH- CHK/IOCHCHK)	177	O (I/I)		C	0 (–/–)	0.0	3.3	3.3	VCC1	VCC5	100
M (IRQ4/IRQ4)	173	O (I/I)		C	0 (–/–)	0.0	3.3	3.3	VCC1	VCC5	100
CP1 [HDRV] (PREQ/IRQ5)	178	O (I/I)		C	0 (–/–)	0.0	0.0	3.3	VCC1	VCC5	100
CP2 [VD0] (BUSY/ IRQ10)	179	O (I/I)		C	0 (–/–)	0.0	0.0	3.3	VCC1	VCC5	100

Table 8. Display Interface (continued)

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
FRM [VDRV] (IRQ12/IRQ12)	181	O (I/I)		C	0 (–/–)	0.0	3.3	3.3	VCC1	VCC5	100
$\overline{\text{LVEE}}$ (IRQ15/ IRQ15)	182	O (I/I)		B	1 (–/–)	3.3	3.3	3.3	VCC1	VCC5	50
$\overline{\text{LVDD}}$ (A12/ BALE)	145	O		E	1(0/1)	3.3	3.3	5.0	VSYS2	VCC5	50
$\overline{\text{IOCS16}}$ [LCDDL0]	196	I [B]		C	– [0]	3.3	3.3	3.3	VCC1	VCC5	70
$\overline{\text{MCS16}}$ [LCDDL1]	197	I [B]		C	– [0]	3.3	3.3	3.3	VCC1	VCC5	70
IRQ14 [LCDDL2]	198	I [B]		C	– [0]	0.0	0.0	0.0	VCC1	VCC5	70
$\overline{\text{SBHE}}$ [LCDDL3]	143	O [B]		C	0[0]	0.0	0.0	0.0	VSYS2	VCC5	70

Notes:

All inputs that have VCC clamp = 5 V are 5 V safe inputs regardless of their VCCIO.

1. *LS in the Clock Off column stands for Last State.*
2. *Reset State Local Bus signal loading 920 mV–0 V. For 33-MHz operation, CPUCLK loading = 30 pF.*

Table 9. Miscellaneous Interface

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
$\overline{\text{IORESET}}$ (1)	140	I		–	–	0.0	0.0	0.0	VCC5	VCC5	
X32IN (2)	201	I		–	–	640 mV	920/0	920/0	AVCC	AVCC	
X32OUT (3)	202	O		osc.	Active	1.68/0	1.68/0	1.68/0	AVCC	AVCC	
LF1	204	A		–	–	1.52	1.52	1.52	AVCC	AVCC	
LF2	205	A		–	–	1.48	1.48	1.48	AVCC	AVCC	
LF3	206	A		–	–	1.52	1.52	1.52	AVCC	AVCC	
LF4	207	A		–	–	1.68	1.68	1.68	AVCC	AVCC	
X1OUT [BAUD_OUT]	200	O		B	(LS) (4)	0.0	1.24	1.24	VCC1	VCC5	50
$\overline{\text{RESIN}}$	141	STI		–	–	0.0	0.0	0.0	VCC	VCC	
SPKR (4)	139	O		B	(LS) (4)	5.0	5.0	5.0	VCC5	VCC5	50
JTAGEN	199	I	PD	–	–	0.0	0.0	0.0	VCC1	VCC5	

Notes:

All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

1. *$\overline{\text{IORESET}}$ (pin #140) requires an external pull-down resistor (~100K).*
2. *Reset State Local Bus signal and Reset State ISA Max signal: 920 mV–0 V frequency = 32 kHz.*
3. *Reset State signal: 1.68 V–0 V frequency = 32 kHz.*
4. *LS in the Clock Off column stands for Last State.*

Table 10. Power Pins

Signal Name	Pin No.	I/O Type	Term	Drive Type	Clock Off	Reset State (volts)			VCCIO	VCC Clamp	Spec. Load (pF)
						Internal CGA	Local Bus	Max ISA			
AVCC (1)	203					3.3	3.3	3.3			
VCC (1)	23, 81, 135,180					3.3	3.3	3.3			
VCC5 (1)	95, 128					5.0	5.0	5.0			
VSYS2 (1)	142					3.3	3.3	5.0			
VSYS (1)	48, 65					5.0	5.0	5.0			
VMEM (1)	9, 22, 35					3.3	3.3	3.3			
VCC1 (1)	176					3.3	3.3	3.3			
GND	1,12, 20, 33, 52, 53, 68, 104, 105, 121, 156, 157, 191, 208										

Notes:
All inputs that have VCC clamp = 5 V are 5-V safe inputs regardless of their VCCIO.

1. *These Reset State entries identify the VCCIO levels that are present on the Am386SC300 device for the three bus mode options. Note that the device is not limited to these VCC levels.*

PIN DESCRIPTIONS

Descriptions of the Am386SC300 microprocessor pins are organized into functional groupings in the following order:

1. Memory Bus
2. System Interface
3. Keyboard Interface
4. Parallel Port Interface
5. Serial Port Interface
6. PCMCIA Interface
7. Power Management Interface
8. Display Interface
9. Miscellaneous Interface
10. Local Bus Interface
11. Maximum ISA Bus Interface
12. JTAG-Boundary Scan Interface
13. Reset and Power

Descriptions of the signals associated with each functional group are given in the following paragraphs.

Memory Bus

$\overline{CAS1H}$–$\overline{CAS1L}$, $\overline{CAS0H}$–$\overline{CAS0L}$, [$\overline{SRCS3}$–$\overline{SRCS0}$]

Column Address Strobe (Outputs; Active Low)

Column Address Strobe indicates to DRAM that a valid column address is present on the MA10–MA0 lines. Two $\overline{CAS}$ signals are allocated to each bank, one per byte.

$\overline{SRCS3}$–$\overline{SRCS0}$ are the alternate pin functions for $\overline{CAS1H}$–$\overline{CAS0L}$ when SRAM is supported instead of DRAM. Each pin selects a byte in one of two SRAM banks. The SRAM functionality is selected via firmware. In this mode, all four of these outputs are active Low.

$\overline{DOSCS}$

DOS ROM Chip Select (Output; Active Low)

The DOS ROM Chip Select is an active Low output that provides the chip select function for the FLASH/ROM array banks that are used to hold the operating system or application code. $\overline{DOSCS}$ is used to select the DOS ROMs and can be configured to respond to direct addressing or Memory Management System (MMS) addressing.

MA11–MA0/SA23–SA12

Memory Address (Outputs; Active High)

Memory Address lines for multiplexed and nonmultiplexed memory devices; their effect depends on the system configuration and the type of bus cycle.

- When system memory is configured as DRAM, the MA10–MA0 are multiplexed outputs and convey the row address during $\overline{RAS}$ assertion and column address during $\overline{CAS}$ assertion.
- When system memory is configured as SRAM, MA11–MA0 are used to convey nonmultiplexed address information during accesses to system memory.
- For cycles that are not targeted to system memory or internal I/O, MA11–MA0 are used to provide non-multiplexed ISA type address signals SA23–SA12, as shown in the following table. See also SA11–SA0.

MA	11	10	9	8	7	6	5	4	3	2	1	0
SA	12	13	23	22	21	20	19	18	17	16	15	14

$\overline{MWE}$

Write Enable (Output; Active Low)

Write Enable is the write command strobe for the DRAM devices.

$\overline{RAS1}$–$\overline{RAS0}$

Row Address Strobe (Output; Active Low)

Row Address Strobe indicates to DRAM that a valid row address is present on the MA11-MA0 lines. One $\overline{RAS}$ signal is allocated for each DRAM bank, one per word.

$\overline{ROMCS}$

BIOS ROM Chip Select (Output; Active Low)

BIOS ROM Chip Select is an active Low output that provides the chip select function for the FLASH/ROM array. $\overline{ROMCS}$ is used to select the BIOS ROM, and can be configured to respond to direct addressing or MMS addressing. When configured for direct addressing, the BIOS ROM can reside at one or all of the following address ranges:

0F0000H–0FFFFFH,
0E0000H–0EFFFFH,
0D0000H–0DFFFFH,
0C0000H–0CFFFFH,
0A0000H–0AFFFFH

The BIOS ROM chip select is also active for accesses into the 64K segment that contains the boot vector, at address FF0000H to FFFFFFH.

0257525 0048573 2T0

System Interface

AEN [TDI]

DMA Address Enable (Output; Active High)

AEN is used to indicate that the current address active on the SA23–SA0 address bus is a memory address, and that the current cycle is a DMA cycle. All I/O devices should use this signal in decoding their I/O addresses, and should not respond when this signal is asserted. When AEN is asserted, the $\overline{\mathrm{DACKx}}$ signals are used to select the appropriate I/O device for the DMA transfer.

This pin is a dual-function pin. When the JTAGEN signal is asserted, this pin functions as the TDI, JTAG Test Data Input pin.

D15–D0

System Data Bus (Bidirectional; Active High)

The System Data Bus inputs data during memory and I/O read cycles, and outputs data during memory and I/O write cycles. During Local Bus and DRAM cycles, this bus represents the CPU data bus.

$\overline{\mathrm{DACK2}}$ [TCLK]

DMA Channel 2 Acknowledge (Output; Active Low)

This output indicates that the current transfer is a DMA transfer to the I/O device connected to this DMA channel. In PC-compatible system designs, this signal can be connected to the Floppy Disk Controller DMA Acknowledge input.

This pin is a dual-function pin. When the JTAGEN signal is asserted, this pin functions as the TCLK (JTAG Test Clock) pin. See the JTAG Interface section for more information on the function of this pin during Test mode.

$\overline{\mathrm{DBUFOE}}$

Data Buffer Output Enable (Output; Active Low)

This output is used to control the output enable on the system data bus buffer. When Low, the outputs of the Data Bus Buffer are enabled.

DRQ2 [TDO]

DMA Channel 2 Request (Input; Active High with Internal Pull Down)

This input is used to request a DMA transfer. It can be connected to the Floppy Disk Controller DMA request output in PC-compatible system designs.

This pin is a dual-function pin. When the JTAGEN signal is asserted, this pin will function as the TDO, JTAG Test Data Out pin. See the JTAG Interface section for more information on the function of this pin during Test mode.

ENDIRH

High Byte Data Buffer Direction Control (Output; Active High)

This output controls the transceiver on the high byte of the data bus, bits 15–8. When asserted, this signal is used to enable the data from the Am386SC300 microprocessor data bus to the buffered data bus.

ENDIRL

Low Byte Data Buffer Direction Control (Output; Active High)

This output controls the transceiver on the low byte of the data bus, bits 7–0. When asserted, this signal is used to enable the data from the Am386SC300 microprocessor data bus to the buffered data bus.

IOCHRDY

I/O Channel Ready (Input; Active High)

This signal is used by ISA slave devices to add wait states to the current transfer. When this signal is deasserted, wait states are added.

$\overline{\mathrm{IOR}}$

I/O Read Command (Output; Active Low)

The $\overline{\mathrm{IOR}}$ signal indicates that the current cycle is a read of the currently selected I/O device. When this signal is asserted, the selected I/O device can drive data onto the data bus.

$\overline{\mathrm{IOW}}$

I/O Write Command (Output; Active Low)

The $\overline{\mathrm{IOW}}$ signal indicates that the current cycle is a write of the currently selected I/O device. When this signal is asserted, the selected I/O device can latch data from the data bus.

IRQ1, IRQ14 [LCDDL2]

Interrupt Request Channels 1 and 14 (Input; Rising Edge/Active High, with Internal Pullup)

This input is connected to the internal 8259A-compatible Interrupt Controller Channels 1 and 14. In PC-compatible systems, IRQ1 may be connected to the 8042 keyboard controller.

(IRQ14 is available unless the internal LCD Controller bus mode is selected and a dual-scan panel interface is selected via firmware.)

$\overline{\mathrm{MEMR}}$

Memory Read Command (Output; Active Low)

The $\overline{\mathrm{MEMR}}$ signal indicates that the current cycle is a read of the currently selected memory device. When this signal is asserted, the selected memory device can drive data onto the data bus.

MEMW

Memory Write Command (Output; Active Low)

The MEMW signal indicates that the current cycle is a write of the currently selected memory device. When this signal is asserted, the selected memory device can latch data from the data bus.

PIRQ1–PIRQ0

Programmable Interrupt Requests (Inputs; Rising Edge/Active High, with Internal Pullup)

These two inputs can be programmed to drive any of the available interrupt controller interrupt request inputs.

MCS16 [LCDDL1]

(Input; Active Low)

This input is used to signal to the ISA control logic that the targeted memory device is a 16-bit device.

(MCS16 is available unless the internal LCD Controller bus mode is selected and a dual-scan LCD panel interface is selected via firmware.)

IOCS16 [LCDDL0]

(Input; Active Low)

This input is used to signal to the ISA control logic that the targeted I/O device is a 16-bit device.

(IOCS16 is available unless the internal LCD Controller bus mode is selected and a dual-scan LCD panel interface is selected via firmware.)

SBHE [LCDDL3]

(Output; Active Low)

Active when the High byte is to be transferred on the upper 8 bits of the data bus.

(SBHE is available unless the internal LCD Controller Bus mode is selected and a dual-scan LCD panel interface is selected via firmware.)

RSTDRV

System Reset (Output; Active High)

This signal is the ISA compatible reset signal. When this signal is asserted, all connected devices reinitialize to their reset state.

SA11–SA0

System Address Bus (Output; Active High)

The System Address Bus outputs the physical memory or I/O port, least-significant, latched addresses. They are used by all external I/O devices and all memory devices other than main system DRAM. During Local Bus cycles, this bus represents the CPU address bus (A11–A1). SA0 is equivalent to A0 during local bus cycles. See MA11–MA0 for SA23–SA12.

SPKR

Speaker, Digital Audio Output (Output)

This signal controls an external speaker driver. It is generated from the internal 8254-compatible Timer Channel 2 output "ANDed" with I/O port 061H, bit 1 (speaker data enable).

TC

Terminal Count (Output; Active High)

This signal is used to indicate that the transfer count for the currently active DMA channel has reached zero, and that the current DMA cycle is the last transfer.

This pin is a dual-function pin. When the JTAGEN signal is asserted, this pin will function as the TMS, JTAG Test Mode Select pin. See the JTAG Interface section for more information on the function of this pin during Test mode.

Keyboard Interface

SYSCLK [XTCLK]

System Clock (Output)

This clock can be used to provide a clock to a keyboard controller. This clock is not synchronous to ISA bus cycles. XTCLK is the XT Keyboard clock.

8042CS [XTDAT]

Keyboard Controller Chip Select (Output; Active Low)

This signal is a decode of A9–A0 = 060H to 06EH, all even addresses. In PC-compatible systems, it connects to the external keyboard controller Chip Select. XTDAT is the XT Keyboard data line.

A20GATE

Address Bit-20 Gate (Input; Active High)

When deasserted, this signal is used to force CPU address bit 20 Low, a function required for PC compatibility. In PC-compatible systems, this signal can be driven by an 8042 keyboard controller, port 2, bit 1.

RC

Reset CPU (Input; Active Low)

This signal resets the internal CPU. In PC-compatible systems, this signal can be driven by a keyboard controller, port 2, bit 0.

Parallel Port Interface

$\overline{\text{ACK}}$

Printer Acknowledge (Input; Active Low)

The printer asserts ACK to confirm that the transfer from the Am386SC300 microprocessor to the parallel port was successful.

$\overline{\text{AFDT}}$ [X14OUT]

Auto Line Feed Detect (Output; Active Low)

Signals the printer to autofeed continuous form paper. This pin can be programmed to become a 14.336-MHz output.

BUSY

Printer Busy (Input; Active High)

The printer asserts BUSY when it is performing an operation.

$\overline{\text{INIT}}$ [$\overline{\text{PCMCWE}}$]

Initialize Printer (Output; Active Low)

This signals the printer to begin an initialization routine. This pin can be programmed to become the PCMCIA write enable signal ($\overline{\text{PCMCWE}}$).

PE

Paper End (Input; Active High)

The printer asserts this signal when it is out of paper.

$\overline{\text{ERROR}}$

(Input; Active Low)

The printer asserts the $\overline{\text{ERROR}}$ signal to inform the parallel port of a deselect condition, PE, or other error condition.

$\overline{\text{PPDWE}}$ [$\overline{\text{PPDCS}}$]

Parallel Port Write Enable (Output; Active Low)

The $\overline{\text{PPDWE}}$ signal is used to control the 374-type latch in a unidirectional parallel port design. To support a bidirectional parallel port design, this pin can be reconfigured ($\overline{\text{PPDCS}}$) to act as an address decode for the parallel port data port. It can then be externally gated with $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ to provide the Parallel Port Data Read and Write Strobes, respectively.

$\overline{\text{PPOEN}}$

Parallel Port Output Buffer Enable (Output; Active Low)

This signal supports a bidirectional parallel port design. This signal is used to control the output enable of the Parallel Port Output Buffer.

SLCT

Printer Select Return (Input; Active High)

The printer asserts SLCT when it has been selected.

$\overline{\text{SLCTIN}}$ [$\overline{\text{PCMCOE}}$]

Printer Selected (Output; Active Low)

Asserting $\overline{\text{SLCTIN}}$ selects the line printer. This pin can be programmed to become the PCMCIA output enable signal ($\overline{\text{PCMCOE}}$).

$\overline{\text{STRB}}$

Strobe (Output; Active Low)

Asserting $\overline{\text{STRB}}$ signals the line printer to latch data currently on the parallel port.

Serial Port Interface

$\overline{\text{CTS}}$

Clear To Send (Input; Active Low)

This signal indicates that the external serial device is ready to accept data.

$\overline{\text{DCD}}$

Data Carrier Detect (Input; Active Low)

This signal indicates that the internal serial port controller has detected a data carrier from the data set of a serial device.

$\overline{\text{DSR}}$

Data Set Ready (Input; Active Low)

This signal is used to indicate that the external serial device is ready to establish a communication link with the internal serial port controller.

$\overline{\text{DTR}}$/CFG1

Data Terminal Ready (Output; Active Low)

This signal indicates to the external serial device that the internal serial port controller is ready to communicate. The state of this signal is used to determine the pin configuration at power-up.

$\overline{\text{RIN}}$

Ring Indicate (Input; Active Low)

This signal is used as a modem control function. A change in state on this signal by the external serial device causes a modem status interrupt. This signal can be used to cause the Am386SC300 microprocessor to resume from a suspended state.

RTS/CFG0

Request To Send (Output; Active Low)

This signal indicates to the external serial device that the internal serial port controller is ready to send data. The state of this signal is used to determine the pin configuration at power-up.

SIN

Serial Data In (Input; Active High)

This signal is used to receive the serial data from the external serial device into the internal serial port controller.

SOUT

Serial Data Out (Output; Active High)

This signal is used to transmit the serial data from the internal serial port controller to the external serial device.

PCMCIA Interface

PCMCOE

Card Memory Output Enable (Output, Active Low)

The Parallel Port SLCTIN signal can be programmed to become PCMCOE. PCMCOE indicates that a memory read cycle from the card I/F is being performed.

PCMCWE

Card Memory Write Enable (Output, Active Low)

The Parallel Port INIT signal can be programmed to become PCMCWE. PCMCWE indicates that a memory write cycle to the card I/F is being performed.

BVD1_A, BVD1_B

Battery Voltage Detect (Inputs)

These signals are generated by the memory card as an indication of the condition of its battery for a memory card interface. For an I/O card interface, these inputs are the cards Status Change Interrupt (active Low).

BVD2_A, BVD2_B

Battery Voltage Detect (Inputs)

These signals are generated by the memory card as an indication of the condition of its battery for a memory card interface. For an I/O card interface, these pins become the speaker inputs from the cards.

CA24

Card Address Bit 24 (Output)

This card address bit is controlled by accessing the Am386SC300 microprocessor configuration registers, and should be connected to the card interface signal A24. This address signal is common to slot A and slot B interfaces.

CA25

Card Address Bit 25 (Output)

This card address bit is controlled by accessing the Am386SC300 microprocessor configuration registers, and should be connected to the card interface signal A25. This address signal is common to slot A and slot B interfaces.

CD_A, CD_B

Card Detect (Inputs; Active Low)

The card detect signals indicate that the card is properly inserted into a socket. These signals should be driven from an "ANDing" of the CD1 and CD2 pins of a single socket. Therefore, two external AND gates are required, one for each slot.

ICDIR

Card Data Direction (Output)

This signal controls the direction of the card data buffers or translators, working in conjunction with the MCEL and MCEH card enable signals to control the data buffers on the card interface. When this signal is High, the data flow is from the Am386SC300 microprocessor to the card socket, indicating a data write cycle. When this signal is Low, the data flow is from the card socket into the Am386SC300 microprocessor, indicating a read cycle. Note that PCMCIA bus buffering may or may not be implemented in a system design.

MCEH_A, MCEH_B

Card Enables, High Byte (Output; Active Low)

These signals enable odd-address bytes for their respective card interfaces.

MCEL_A, MCEL_B

Card Enables, Low Byte (Output; Active Low)

These signals enable even-address bytes for their respective card interfaces.

RDY_A, RDY_B

Card Ready (Inputs; Active High)

This signal indicates that the respective card is ready to accept a new data transfer command if a memory interface is selected. If the card interface is configured as an I/O interface, this signal is used as the card Interrupt Request input into the Am386SC300 microprocessor (active High).

REG_A, REG_B

Attribute Memory Select (Output; Active Low)

This signal selects either the Attribute Memory or the Common Memory. This signal will be inactive (High) for accesses to Common Memory, and asserted (Low) for accesses to Attribute Memory. This signal is also asserted (Low) for all I/O accesses.

RST_A, RST_B

Card Reset (Outputs; Active High)

These signals reset their respective cards. When active, this signal clears the Card Configuration Option Register, thus placing a card in a Memory Only mode.

VPP_A, VPP_B

Program and Peripheral Voltage Control (Output; Active High)

These signals can be used to enable the programming voltages to their respective card interfaces.

WAIT_AB

Extend Bus Cycle (Input; Active Low)

This signal delays the completion of the memory access or I/O access that is currently in progress. When this signal is asserted (Low), wait states will be inserted into the cycle in progress. A two-card solution needs each slot's WAIT_AB signal "ANDed" before being input to the Am386SC300 device.

WP_A, WP_B

Write Protect (Inputs; Active High)

When a memory interface is selected, this signal indicates the status of the respective card's Write Protect Switch. When the respective card is configured for an I/O interface, this signal is used to indicate that the currently accessed port is a 16-bit port (IOCS16 active Low).

Power Management Interface

ACIN

AC Supply Active (Input; Active High)

When asserted, this signal disables all power management functions (if so enabled). It can be used to indicate when the system is being supplied power from an AC source.

BL4–BL1

Battery Low Detects (Inputs; Negative Edge Sensitive)

These signals are used to indicate to the Am386SC300 microprocessor the current status of the battery. BL4–BL1 can indicate various conditions of the battery as status changes. A High indicates normal operating conditions, while a Low indicates a low voltage warning condition. These inputs can be used to force the system into one of the power saving modes when activated, as follows:

- BL1 can be programmed to force the system to go to Low Speed PLL mode or to generate an SMI.
- BL2 can be programmed to force the system to Sleep mode if not already in Sleep, or to generate an SMI.
- BL3 can only be programmed to generate an SMI.
- BL4 can be programmed to force the system to Suspend mode.

EXTSMI

External System Management Interrupt (Input; Edge Sensitive)

This input is provided to allow external logic to generate an SMI request to the CPU. This input is edge triggered, with the polarity programmable.

LPH

Latched Power Control (Output; Active Low)

This signal is the inverse of BL4 if ACIN is not true, and BL4 is enabled.

PGP3–PGP0

Programmable Chip Select Generation (Input/Output)

PGP0 and PGP1 can be programmed as input or output. The default is input. PGP2 and PGP3 are output only.

These general purpose pins can be individually programmed as decoder outputs or chip selects for other external peripheral devices.

PGP0 and PGP2 can be gated with I/O Write or act as an address decode only. PGP1 and PGP3 can be gated with I/O Read or act as an address decode only. PGP0 and PGP1 can be directly controlled via a single register bit if configured to do so. PGP2 and PGP3 can also be configured for a specific state when the PMU state is in the Off state.

PMC4–PMC0

Power Management Controls (Output; Programmable)

Power Management Control outputs control the power to various external devices and system components. The PMC0, PMC1, PMC2, and PMC4 signals are asserted Low immediately after reset, and the PMC3 signal is asserted High immediately after reset. Each of the PMC pins can then be programmed to be High or Low for each of the Am386SC300 microprocessor power management modes.

$\overline{\text{SUS/RES}}$

Suspend/Resume Operation (Input; Rising Edge)

When the Am386SC300 microprocessor is in High Speed PLL, Low Speed PLL, or Doze mode, a positive edge on this pin causes the internal logic to step down through the Power Management modes (one per refresh cycle) until Sleep mode is entered. If in Sleep, Suspend, or Off mode, a positive edge on this pin causes the Am386SC300 microprocessor to enter the High Speed PLL mode.

Display Interface

The signals listed as part of the "Display Interface" are only available when the Am386SC300 microprocessor is configured with the internal LCD controller enabled. If the internal LCD controller is disabled, the functions of these pins change to support either a CPU Local Bus Interface or maximum ISA bus.

CP1 [HDRV]

LCD Panel Line Clock or HSYNC (Output)

This is the Line Clock when in internal LCD mode, and an LCD configuration is selected. It is activated at the start of every pixel line refresh cycle.

This signal is the Horizontal Synch if a CRT configuration is selected. This function is selected via firmware.

CP2 [VD0]

LCD Panel Shift Clock (Output)

This is the nibble/byte strobe when in internal LCD mode, and an LCD configuration is selected. It is used by the LCD to latch data.

This is the dot clock if a CRT configuration is selected. This function is selected via firmware.

$\overline{\text{DSCE}}$

Display SRAM Chip Enable (Output; Active Low)

This signal generates the external video SRAM Chip Enable.

DSMA14–DSMA0

Display SRAM Address Bus (Output)

These signals generate the address to the SRAM. Up to 32 Kbytes can be supported for the display interface.

DSMD7–DSMD0

Display SRAM Data Bus (Bidirectional)

These signals provide the data bus used for the video SRAM.

$\overline{\text{DSOE}}$

Display SRAM Output Enable (Output; Active Low)

This signal controls the video SRAM Output Enable pin.

$\overline{\text{DSWE}}$

Display SRAM Write Enable (Output; Active Low)

When asserted, this signal indicates a Write to the video SRAM.

FRM [VDRV]

LCD Panel Line Frame Start or VSYNC (Output)

This signal is asserted at the start of every frame (panel scan) when in LCD mode, and an LCD configuration is selected.

This signal is the Vertical Synch in CRT mode. This function is selected via firmware.

LCDD0 [R]

LCD Data Bit 0/CRT Red (Output)

When in internal LCD mode, and an LCD configuration is selected, this signal is data bit 0.

This signal, when configured for CRT mode, generates a CGA-compatible Red signal. This function is selected via firmware.

LCDD1 [G]

LCD Data Bit 1/CRT Green (Output)

When in internal LCD mode, and an LCD configuration is selected, this signal is data bit 1.

This signal, when configured for CRT mode generates a CGA-compatible Green signal. This function is selected via firmware.

LCDD2 [B]

LCD Data Bit 2/CRT Blue (Output)

When in internal LCD mode, and an LCD configuration is selected, this signal is data bit 2.

This signal, when configured for CRT mode, generates a CGA-compatible Blue signal. This function is selected via firmware.

LCDD3 [I]

LCD Data Bit 3/CRT Intensity (Output)

When in internal LCD mode, and an LCD configuration is selected, this signal is data bit 3.

This signal, when configured for CRT mode, generates a CGA-compatible Intensity signal. This function is selected via firmware.

[LCDDL3–LCDDL0]

LCD Panel Data Bits for Dual-Scan Panels (Outputs)

When the Am386SC300 microprocessor is programmed to support LCD Dual-Scan Panel mode (separate data bits for the top and bottom half of the panel), these bits (LCDDL3–LCDDL0) are for the bottom half of the screen. LCDD3–LCDD0 are the data bits for the top half of the screen. LCD Dual-Scan Panel mode is selected via firmware.

$\overline{\text{LVDD}}$

LCD Panel VDD Voltage Control (Output; Active Low)

This signal is used to control the assertion of the LCD's VDD driver. $\overline{\text{LVDD}}$ is provided to be part of the solution in sequencing the panel's VDD, DATA, and VEE signals in the proper order.

$\overline{\text{LVEE}}$

LCD Panel VEE Voltage Control (Output; Active Low)

This signal is used to control the assertion of the LCD's VEE driver. $\overline{\text{LVEE}}$ is provided to be part of the solution in sequencing the panel's VDD, DATA, and VEE signals in the proper order.

M

LCD Panel AC Modulation (Output)

In internal LCD mode, this is the AC modulation signal for the LCD. AC modulation causes the LCD to change polarity on its crystal material to keep the LCD from forming a DC bias.

Miscellaneous Interface

LF1, LF2, LF3, LF4 (Analog inputs)

Loop Filters

These pins are used to connect external components that make up the loop filters for the internal PLLs.

X1OUT [BAUD-OUT]

14-MHz/UART Output

This can be programmed to be either the 14.336-MHz clock or the serial baud rate clock for serial infrared devices. The 14.336-MHz output can be used by external video controllers. As BAUD_OUT, it is 16 x the bit data rate of the serial port and is used by serial infrared devices.

X14OUT

14-MHz Output

The Parallel Port $\overline{\text{AFDT}}$ output can be programmed to become X14OUT, a 14.336-MHz clock.

X32IN, X32OUT

32.768-kHz Crystal Interface

These pins are used for the 32.768-kHz crystal. This is the main clock source for the Am386SC300 microprocessor and is used to drive the internal Phase-Locked Loops that generate all other clock frequencies needed in the system.

Local Bus Interface

The Local Bus Interface pins are only available when the Am386SC300 microprocessor's internal LCD controller is disabled and the Am386SC300 microprocessor pin configuration is set to support a CPU local bus and a partial ISA bus. The following list of pins is specific to local bus functionality. In Local Bus mode, additional ISA pins are also available. These pins are described in the next section "Maximum ISA Bus Interface" because these pins are available in both Local Bus and Maximum ISA Bus modes.

$\overline{\text{387ERR}}$

Numeric Coprocessor Error (Input; Active Low)

This signal is used to allow the interface of an 80387-compatible coprocessor. It is available only when local bus is enabled. This should be pulled up externally in local bus mode if not connected to a coprocessor.

387RESET

Numeric Coprocessor Reset (Output; Active High)

This signal is used to allow the interface of an 80387-compatible coprocessor. It is available only when local bus is enabled.

$\overline{\text{ADS}}$

Local Bus Address Strobe (Output; Active Low)

Local Bus Address Strobe is an active Low address strobe signal for 386 local bus devices.

$\overline{\text{BHE}}$

Local Bus Byte High Enable (Output; Active Low)

This signal indicates to the local bus devices that data is being transferred on the high byte of the data bus.

$\overline{\text{BLE}}$

Local Bus Byte Low Enable (Output; Active Low)

This signal indicates to the local bus devices that data is being transferred on the low byte of the data bus.

0257525 0048580 430

$\overline{\text{BUSY}}$

387 Busy (Input; Active Low)

This signal is used by the 387 to signal its status as busy. This should be pulled up externally in Local Bus mode if not connected to a coprocessor.

CPUCLK

CPU 2X Clock (Output)

This is the timing reference for the local bus device.

$\overline{\text{CPURDY}}$

386 CPU Ready Signal (Output; Active Low)

This signal shows the current state of the 386 core CPU's $\overline{\text{CPURDY}}$ signal.

CPURST

CPU Reset (Output; Active High)

This signal is used to force the local bus device to an initial condition. It is also used to allow the Local Bus device to synchronize to the CPUCLK. This signal is taken directly from the internal CPU reset.

D/$\overline{\text{C}}$

Local Bus Data/Control (Output; Active Low)

This signal indicates to the local bus devices that the current cycle is either a Data cycle or a Control cycle. A Low on this signal indicates that the current cycle is a Control cycle.

$\overline{\text{LDEV}}$

Local Bus Device Select (Input; Active Low)

This signal is used by the local bus devices to signal that they will respond to the current cycle.

$\overline{\text{LRDY}}$

Local Bus Device Ready (Input; Active Low)

This signal is used by the local bus devices to terminate the current bus cycle.

M/$\overline{\text{IO}}$

Local Bus Memory/I/O (Output; Active Low)

This signal indicates to the local bus devices that the current cycle is either a memory or an I/O cycle. A Low on this signal indicates that the current cycle is an I/O cycle.

PREQ

Processor Request (Input; Active High)

This signal is used by the 387 to request the CPU. This should be pulled down externally in Local Bus mode if an external coprocessor is not present.

W/$\overline{\text{R}}$

Local Bus Write/Read (Output; Active Low)

This signal indicates to the local bus devices that the current cycle is either a Read or a Write cycle. A Low on this signal indicates that the current cycle is a Read cycle.

A23–A12

Local Bus Upper Address Lines (Output)

These signals are the local bus CPU address lines when in Local Bus mode. These signals are combined with the SA11–SA0 signals to form the complete CPU address bus during local bus cycles.

Maximum ISA Bus Interface

The pins listed below as part of the "ISA Bus Interface" are only available when the Am386SC300 microprocessor pin configuration is configured to enable the maximum ISA Bus. When the maximum ISA Bus Interface is enabled, the internal LCD controller and the CPU Local Bus interface are disabled. (This mode does not support Master and ISA refresh cycles.)

$\overline{\text{0WS}}$

Zero Wait State (Input; Active Low)

This input can be driven active by an ISA memory device to indicate that it can accept a Zero Wait State memory cycle.

BALE

Bus Address Latch Enable (Output; Active High)

This PC/AT-compatible signal is used by external devices to latch the LA signals for the current cycle.

$\overline{\text{DACK7}}$, $\overline{\text{DACK6}}$, $\overline{\text{DACK5}}$, $\overline{\text{DACK3}}$, $\overline{\text{DACK2}}$, $\overline{\text{DACK1}}$, $\overline{\text{DACK0}}$

DMA Acknowledge (Output; Active Low)

DMA Acknowledge signals are active Low output pins that acknowledge their corresponding DMA requests.

Note: *The $\overline{\text{DACK2}}$ signal is available regardless of the bus mode the Am386SC300 microprocessor is in. $\overline{\text{DACK1}}$ and $\overline{\text{DACK5}}$ are also available in the Local Bus pin configuration.*

DRQ7, DRQ6, DRQ5, DRQ3, DRQ2, DRQ1, DRQ0

DMA Request (Input; Active High)

DMA Request signals are asynchronous DMA channel request inputs used by peripheral devices to gain access to a DMA service.

Note: *The DRQ2 signal is available regardless of the Am386SC300 device's bus mode. DRQ1 and DRQ5 are also available in the Local Bus pin configuration.*

$\overline{\text{IOCHCHK}}$

I/O Channel Check (Input; Active Low)

This signal is a PC/AT-compatible signal used to generate an NMI or SMI.

Note: *$\overline{\text{IOCHCHK}}$ is also available in the Local Bus pin configuration.*

IRQ15, IRQ12–IRQ9, IRQ7, IRQ5, IRQ4

Interrupt Request
(Inputs; Rising Edge/Active High Trigger)

Interrupt Request input pins signal the internal 8259-compatible interrupt controller that an I/O device needs servicing.

Note: *IRQ4, IRQ12, and IRQ15 are also available in the Local Bus pin configuration*

LA23–LA17

Latchable ISA Address Bus (Outputs)

These are the ISA latchable address signals. These signals are valid early in the bus cycle so that external peripherals may have time to decode the address and return certain control feedback signals such as $\overline{\text{MCS16}}$.

$\overline{\text{LMEG}}$

Address is in Low Meg (Output; Active Low)

This signal is active (Low) whenever the address for the current cycle is in the first Mbyte of memory address space (SA23 = SA22 = SA21 = SA20 = 0). This output can be used to allow generation of the $\overline{\text{SMEMR}}$ and $\overline{\text{SMEMW}}$ signals for PC/AT compatibility.

JTAG-Boundary Scan Interface

The JTAG pins described here are shared pin functions. The JTAG pin functions are enabled by the JTAGEN signal.

JTAGEN

JTAG Enable (Input; Active High)

This pin enables the JTAG pin functions. When this pin is High, the JTAG interface is enabled. When this pin is Low, the JTAG pin functions are disabled and the pins are configured to their default functions. See the Pin Designations, System Interface, and Miscellaneous Interface tables for the JTAG pin default function descriptions.

TCK

Test Clock (Input)

Test Clock is a JTAG input clock, which is used to access the Test Access Port.

TDI

Test Data Input (Input)

Test Data Input is the serial input stream for JTAG scan input data.

TDO

Test Data Output (3-State Output)

Test Data Output is the serial output stream for JTAG scan result data.

TMS

Test Mode Select (Input)

Test Mode Select is an input for controlling the Test Access Port.

Reset and Power

AVCC

3.3-V Supply Pins

These supply pins provide power to the analog section of the Am386SC300 microprocessor's internal PLLs. Extreme care should be taken that this supply voltage is isolated properly to provide a clean, noise-free voltage to the PLLs.

GND

System Ground Pins

These pins provide electric grounding to the analog section of the Am386SC300 microprocessor's internal PLLs.

$\overline{\text{RESIN}}$

Master Reset (Input; Active Low)

$\overline{\text{RESIN}}$ indicates that power is being applied to the AM386SC300 device. When this signal is asserted, the RTC and Interval registers are reset.

0257525 0048582 203

IORESET

Reset Input (Input; Active Low)

IORESET is an asynchronous hardware reset input equivalent to POWERGOOD in the AT-system architecture. Asserting this signal does not reset the RTC RAM invalid bit.

VCC

3.3-V DC Supply Pins

These supply pins provide power to the Am386SC300 microprocessor core. Refer to AC Characteristics for VCC power up timing restrictions.

VCC1

3.3-V or 5-V Supply Pin

This supply pin provides power to a subset of the LCD/alternate, power management, and ISA interface pins.

VCC5

5-V DC Supply Pins

These supply pins provide power to the 5-V only interface pins. These pins could be 3.3 V in a pure 3.3-V system.

VMEM

3.3-V or 5-V Supply Pins

These supply pins provide power to the Memory Interface and Data Bus pins (D15–D0). These pins must be connected to the same DC supply as the system DRAMs.

VSYS

3.3-V or 5-V Supply Pins

These supply pins provide power to a subset of the ISA address and command signal pins, in addition to external memory chip selects and buffer direction controls and other miscellaneous functions.

VSYS2

3.3-V or 5-V Supply Pins

These supply pins provide power to some of the Am386SC300 microprocessor alternate system interface pins.

FUNCTIONAL DESCRIPTION

The Am386SC300 microprocessor architecture consists of several components, as shown in the device block diagram. These components can be grouped into eight main functional modules:

1. The Am386SXLV microprocessor core itself, including SMM power management hardware
2. A memory controller and associated mapping hardware
3. Two PCMCIA, Revision 2.1 slots
4. An additional power management controller that interfaces to the CPU's System Management Mode (SMM) and is integrated tightly with internal clock generator hardware
5. Core peripheral controllers (DMA, interrupt controller, and timer)
6. Additional peripheral controllers (UART, parallel port, and real-time clock)
7. AT support features
8. An integrated LCD controller, optional local bus controller, or optional maximum ISA bus

The remainder of this section describes these modules.

Am386SXLV CPU Core

The CPU core component is a full implementation of the AMD Am386SXLV 32-bit low-voltage microprocessor (with I/O pads removed).

Along with standard 386 architectural features, the CPU core includes SMM. SMM and the other features of the CPU are described in the *3-Volt System Logic for Personal Computers – AMD Order Number 17028.*

Memory Controller

The Am386SC300 microprocessor memory controller is a unified control unit that supports a high-performance 16-bit data path to DRAM or SRAM. No external memory bus buffers are required, and up to 16 Mbytes in two 16-bit banks can be supported. The System Block Diagram, Figure 7 on page 52, shows a typical palm-top memory configuration.

The Am386SC300 microprocessor's memory controller supports an EMS-compatible Memory Mapping System (MMS) with 12 page registers. This facility can be used to provide access to ROM-based software. MMS is also used in the PCMCIA slot support. Shadow RAM is also supported.

The Memory Controller supports one of three different memory operating modes: SRAM, Page mode DRAM, or Enhanced Page mode DRAM. Enhanced Page mode increases DRAM access performance by effectively increasing the DRAM page size in a two-bank DRAM system.

The memory controller operation is synchronous with respect to the CPU. This ensures maximum performance for all transfers to local memory. The clock stretching implemented by the clock generation circuitry works to reduce synchronous logic power consumption.

As shown in the table below, the two DRAM operating modes are defined by the MOD field in the Memory Configuration Register, Index 66H, bits 1 and 0.

DRAM Mode Selection

MOD0 (Index 66H, bit 0)	Function
0	Page mode
1	Enhanced Page mode

The Am386SC300 device defaults to a DRAM interface. The SRAM mode is selected via bit 0 of the Switch 2 Register, Index 70H. The memory controller provides for a direct connection of two 16-bit banks supporting up to 16 Mbytes of DRAM, utilizing industry standard modules. The Am386SC300 device shares the DRAM address lines MA0–MA11 with the upper system address lines SA12–SA23 in order to reduce pin count. This signal sharing is shown in the table below.

MA and SA Signal Pin Sharing

System Address	Memory Address
SA23–SA14	MA9–MA0
SA13	MA10
SA12	MA11

The Am386SC300 device also shares the DRAM data bus with the system data bus on the D15–D0 pins. In a typical system, an SD bus is created with an external x 16 bit buffer or level translator to isolate the DRAM data bus from the rest of the system. Refer to the Typical System Block Diagram, Figure 7, on page 52 of this data sheet. The DRAM configurations are supported as shown in Table 11 below. Note that the configurations that use 512 Kbyte x 8 bit and 1 Mbyte x 16 bit DRAMs employ asymmetrical addressing. Tables 12 and 13, on the following page, show the relationship of the CPU address mapped to the DRAM memory.

Table 11. Supported DRAM Configuration

			Index B1H		Index B4H	Index Reg. 66H		
Total DRAM Size	Bank 0 DRAMs	Bank 1 DRAMs	Bit 7	Bit 6	Bit 7	Bit 4	Bit 3	Bit 2
512 Kbyte	4 256 Kbyte x 4 bits	–	0	0	1	x	x	x
1 Mbyte	4 256 Kbyte x 4 bits	4 256 Kbyte x 4 bits	0	1	1	x	x	x
1 Mbyte	2 512 Kbyte x 8 bits	–	x	x	0	0	0	1
2 Mbyte	2 512 Kbyte x 8 bits	2 512 Kbyte x 8 bits	x	x	0	0	1	0
2 Mbyte	4 1 Mbyte x 4 bits	–	x	x	0	0	1	1
2 Mbyte	1 1 Mbyte x 16 bits		1	0	1	x	x	x
4 Mbyte	4 1 Mbyte x 4 bits,	4 1 Mbyte x 4 bits	x	x	0	1	0	0
4 Mbyte	1 1 Mbyte x 16 bits	1 1 Mbyte x 16 bits	1	1	1	x	x	x
8 Mbyte	4 4 Mbyte x 4 bits	–	x	x	0	1	0	1
16 Mbyte	4 4 Mbyte x 4 bits	4 4 Mbyte x 4 bits	x	x	0	1	1	0

Table 12. DRAM Address Translation (Page Mode)

Index B4H Bit 7	Index 66H Bits 4 3 2	Index B1H Bits 7 6	DRAM Size (Byte)	DRAM Bank 0 (Byte)	DRAM Bank 1 (Byte)	RAS CAS	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
0	0 0 1	x x	1M	1M	–	RAS	–	–	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
						CAS	–	–	–	A9	A8	A7	A6	A5	A4	A3	A2	A1
0	0 1 0	x x	2M	1M	1M	RAS	–	–	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
						CAS	–	–	–	A9	A8	A7	A6	A5	A4	A3	A2	A1
0	0 1 1	x x	2M	2M	–	RAS	–	–	A19	A18	A17	A16	A15	A14	A13	A12	A11	A20
						CAS	–	–	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
0	1 0 0	x x	4M	2M	2M	RAS	–	–	A19	A18	A17	A16	A15	A14	A13	A12	A11	A20
						CAS	–	–	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
0	1 0 1	x x	8M	8M	–	RAS	–	A22	A19	A18	A17	A16	A15	A14	A13	A12	A21	A20
						CAS	–	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
0	1 1 0	x x	16M	8M	8M	RAS	–	A22	A19	A18	A17	A16	A15	A14	A13	A12	A21	A20
						CAS	–	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
1	x x x	0 0	512K	512K	–	RAS	–	–	–	A18	A17	A16	A15	A14	A13	A12	A11	A10
						CAS	–	–	–	A9	A8	A7	A6	A5	A4	A3	A2	A1
1	x x x	0 1	1M	512K	512K	RAS	–	–	–	A18	A17	A16	A15	A14	A13	A12	A11	A10
						CAS	–	–	–	A9	A8	A7	A6	A5	A4	A3	A2	A1
1	x x x	1 0	2M	2M	–	RAS	A20	A9	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
						CAS	–	–	–	–	A8	A7	A6	A5	A4	A3	A2	A1

Note:

Page mode DRAM using two banks of 1 Mbyte x 16 DRAMS is not supported. Use Enhanced Page mode for two bank configuration.

Table 13. DRAM Address Translation (Enhanced Page Mode)

Index B4H Bit 7	Index 66H Bits 4 3 2	Index B1H Bits 7 6	DRAM Size (Byte)	DRAM Bank 0 (Byte)	DRAM Bank 1 (Byte)	RAS CAS	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
0	0 1 0	x x	2M	1M	1M	RAS	–	–	A19	A18	A17	A16	A15	A14	A13	A12	A11	A20
						CAS	–	–	–	A9	A8	A7	A6	A5	A4	A3	A2	A1
0	1 0 0	x x	4M	2M	2M	RAS	–	–	A19	A18	A17	A16	A15	A14	A13	A12	A21	A20
						CAS	–	–	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
0	1 1 0	x x	16M	8M	8M	RAS	–	A22	A19	A18	A17	A16	A15	A14	A13	A23	A21	A20
						CAS	–	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
1	x x x	0 1	1M	512K	512K	RAS	–	–	–	A18	A17	A16	A15	A14	A13	A12	A11	A19
						CAS	–	–	–	A9	A8	A7	A6	A5	A4	A3	A2	A1
1	x x x	1 1	4M	2M	2M	RAS	A20	A21	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
						CAS	–	–	–	–	A8	A7	A6	A5	A4	A3	A2	A1

Notes:

1. *See Table 11 for a description of the physical DRAM devices supported.*
2. *Bit 0 of the Memory Configuration Register, Index 66H must be set to enable Enhanced Page mode.*
3. *Bit 4 of the Version Register, Index 64H must be set for 2 Mbyte Enhanced Page mode only.*

In the case of SRAMs, up to 16 Mbytes can be accessed, the SRAM being organized as one or two banks. Each bank is 16 bits wide, and is provided with a Low and High byte select.

An SRAM memory interface is selected by setting bit 0 of the Switch 2 Register, Index 70H. If this is done, $\overline{\text{CAS1H}}$, $\overline{\text{CAS1L}}$, $\overline{\text{CAS0H}}$, and $\overline{\text{CAS0L}}$ will have their alternate function as SRAM chip select pins 3–0 ($\overline{\text{SRCS3}}$–$\overline{\text{SRCS0}}$). The table below shows the key SRAM access pins.

SRAM Access Pins

Pin Name	I/O	Function
$\overline{\text{SRCS0}}$	O	SRAM Bank 0 Low Byte Select
$\overline{\text{SRCS1}}$	O	SRAM Bank 0 High Byte Select
$\overline{\text{SRCS2}}$	O	SRAM Bank 1 Low Byte Select
$\overline{\text{SRCS3}}$	O	SRAM Bank 1 High Byte Select
SA	O	Address

The MS2–MS0 bits in the Memory Configuration Register, Index 66H, are also used to program the total SRAM size. Bit 7 of the PCMCIA Setup Register, Index B4H, must be cleared.

PCMCIA Slots

The Am386SC300 microprocessor supports two Revision 2.1 PCMCIA slots.

MMS mapping logic is used to access the PCMCIA memory address space. Up to twelve 16-Kbyte pages of the CPU's address space are mapped into windows of PCMCIA memory address space.

Depending on the system requirements, the address and data lines to the PCMCIA slots may or may not require external buffers (see the Typical System Block Diagram).

The PMU Modes and Clock Generators

The Power Management Unit (PMU) monitors all system activities (e.g., keyboard, screen, and disk events), and, based on the state of the system, determines in which *operating mode* the system should be running. The PMU supports six operating modes, each defined by a different combination of CPU and peripheral operation, as shown in the list that follows.

1. **High Speed PLL.** All clocks are at fastest speed and all peripherals powered up. This is the mode the system enters when activity is detected by the PMU.
2. **Low Speed PLL.** The internal 2x CPU clock is reduced to a maximum of 4.608 MHz. All other clocks and peripherals operate at full speed. This is the first level of power conservation; it is entered after a specified elapsed time with no activity.
3. **Doze.** The second level of power conservation. The CPU, system, and DMA clocks are stopped. The High Speed PLL is turned off. This mode is entered after a specified elapsed time with no activity.
4. **Sleep.** Additional clocks and peripherals are stopped after additional inactivity has been detected. The exact parameters can be programmed. The Low Speed PLL can be left on, so a quick startup is possible.
5. **Suspend.** Virtually all of the system is shut down, including all clocks, the 8254 timer, and the phase locked loops (a programmable recovery time is associated with this mode). The 32.768-kHz clock input is still running.
6. **Off.** This level is virtually the same as Suspend. Two outputs can be programmed to change state when the transition from Suspend to Off occurs. DRAM refresh can be disabled in OFF mode.

In addition, the Am386SC300 microprocessor can manage the power consumption of peripheral devices. This control can be forced upon entering a specific operating mode or it can be handled directly by firmware. The Am386SC300 microprocessor PMU controls five Power Management Control (PMC) pins that are controlled by the operating modes.

Clock Generation

The Am386SC300 microprocessor requires only one 32.768-kHz clock input that is used to generate all other clock frequencies required by the system. This 32.768-kHz clock input is provided through the X32IN and X32OUT pins and crystal oscillator circuit. This input frequency is then used to internally drive multiple Phase Locked Loops that create all necessary frequencies.

The clock rate that is used to drive the internal CPU is determined by the mode of operation of the Am386SC300 microprocessor.

The clock generation, control, and distribution scheme are detailed in Figures 1 and 2, which follow.

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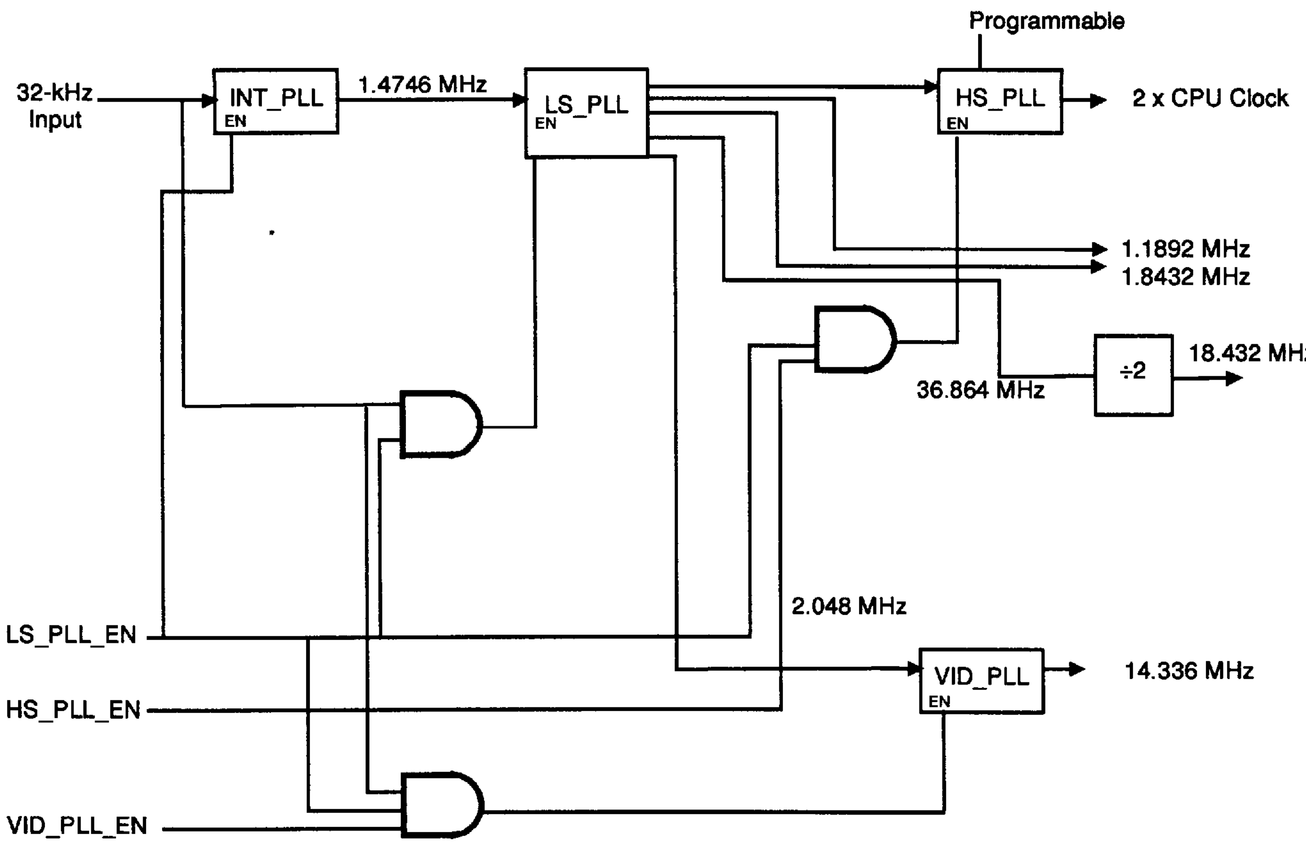

Figure 1. PLL Block Diagram

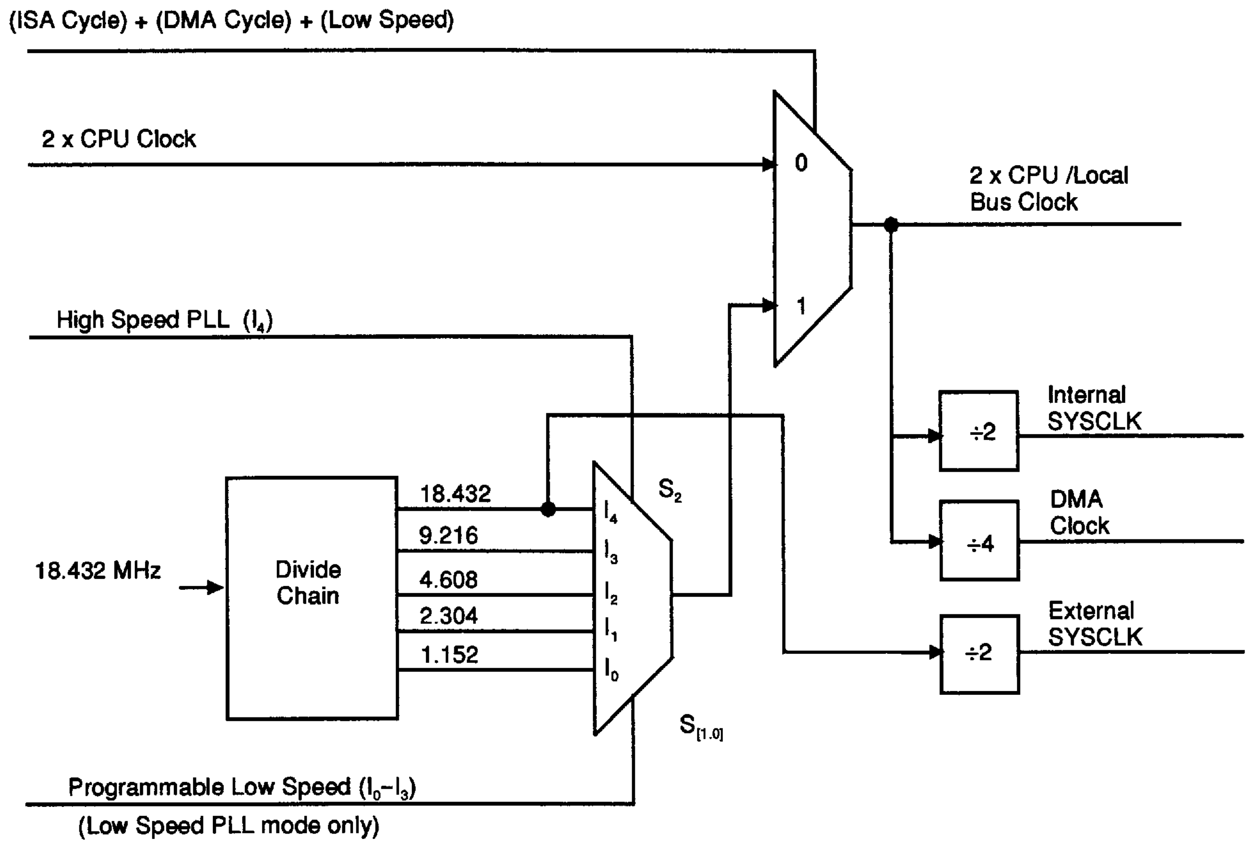

Figure 2. Clock Steering Block Diagram

In the PLL Block Diagram, the INT_PLL is the Intermediate PLL, and is used to multiply the 32.768-kHz input frequency by 45 to produce a 1.4746-MHz input for use by the LS_PLL and the VID_PLL. The LS_PLL, or Low Speed PLL, is used to again multiply the 1.4746-MHz input by 25 to produce a 36.864-MHz output. This output of the LS_PLL is then divided down to provide the frequencies shown in the table below.

The LS_PLL also generates a 2.048-MHz signal used by the VID_PLL or Video PLL to generate the 14.336-MHz clock used by the internal LCD Controller. This frequency is also available on the X1OUT pin for use by an external video controller if selected.

The HS_PLL can be programmed to provide one of the following high speed CPU clock frequencies:

2 x CPU Frequency	HS_PLL Output Frequency
40 MHz	39.496 MHz
50 MHz	50.023 MHz
66 MHz	65.829 MHz

Am386SC300 Microprocessor Power Management

Dynamic CPU clock switching is the primary form of power management in the Am386SC300 microprocessor. When the system is in the High Speed PLL mode, the Élan device can be configured to use the High Speed clock output of the PLL for main memory, local bus accesses, CPU idle cycles, and ROM accesses configured to use the High Speed Clock. During cycles to I/O devices, PCMCIA, ROM, and other external ISA devices, the CPU clock is dynamically switched to the output of the Low Speed PLL.

During operation in Low Speed PLL mode, the CPU clock is driven from Low Speed clock output of the Low Speed PLL divide chain. The CPU clock frequency used during Low Speed mode is programmable to the following frequencies: 4.608 MHz, 2.304 MHz, 1.152 MHz, and 0.567 MHz. During Doze, Sleep, and Suspend modes of operation, the CPU clock is normally stopped. This clock operates at 9.216 MHz when it is running.

Slow refresh and self refresh DRAMs are supported by the Am386SC300 microprocessor. The refresh timer source and the refresh rate are selectable. When the CPU clock is stopped, the only clock source for refresh is the 32-kHz clock. $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ DRAM refresh is performed.

When the DMA sub-system is idle, the DMA clock control logic stops the clock input to the DMA controllers. The DMA clock is started whenever any of the DREQ inputs go High. Once the DMA cycle is in progress, the DMA clock remains active as long as a DREQ input is High or the internal AEN signal is active.

To reduce power consumption in Doze, Sleep, and Suspend modes, the CPU clock is turned off. To further reduce the power consumption in these three modes, the High Speed PLL is shut off. The Low Speed PLL is left on by default, but can be programmed to turn off in all three modes.

Table 14. PLL Output

Phase Locked Loops	Frequency	Where Used
INT_PLL	1.4746 MHz	LS_PLL and VID_PLL
LS_PLL	36.864 MHz	Divide by 2
	1.8432 MHz	16450 UART clock
	1.1892 MHz	8254 Timer clock
HS_PLL	39.496 MHz, 50.023 MHz, or 65.829 MHz	Input to high speed/low speed MUX
VID_PLL	14.336 MHz	LCD Controller

Table 15. PMU Modes

Mode	Description
Power On	After Power on reset, system enters High Speed PLL mode.
High Speed PLL	The system will be in this mode as long as activities are detected by activity monitor (described in the Programmable Activity Mask Registers, Index 08H, 75H, and 76H).
Low Speed PLL	The system will enter this mode from High Speed PLL mode, after a programmable 1/512 s to 1/2 s, or 1/16 s to 16 s of inactivity.
Doze	The system will enter this mode from Low Speed PLL mode, after a programmable 1/16 s to 16 s, or 1/2 s to 128 s of inactivity.
Sleep	The system will enter this mode from Doze mode, after a programmable 4 s to 17 minutes of inactivity.
Suspend	The system will enter this mode from Sleep mode, after a programmable 1/16 s to 16 s of inactivity.
Off	The system will enter this mode from Suspend mode after a programmable 1 to 256 minutes of inactivity.

Table 16. Internal Clock States

Mode	High-Speed CPU CLK	Low-Speed CPU CLK	VIDEO CLK	DMA CLK	SYSCLK	8254 CLK (Timer)	16450 CLK (UART)
High Speed PLL	33/25/20/9.2 MHz	9.2 MHz	14.336 MHz	4.6 MHz	9.2 MHz	1.19 MHz	1.8432 MHz
Low Speed PLL	4.608/2.304/ 1.152/0.567 MHz	4.608/2.304/ 1.152/0.567 MHz	14.336 MHz	2.3/1.2/ 0.58/0.29 MHz	9.2 MHz	1.19 MHz	1.8432 MHz
Doze	DC[1]	DC[1]	14.3 MHz/DC[2]	DC[1]	9.2 MHz/DC[2]	1.19 MHz/DC[2]	1.8 MHz/DC[2]
Sleep	DC	9.2 MHz/DC[4]	14.3 MHz/DC[2]	4.6 MHz/DC[4]	DC	1.19 MHz/DC[2]	1.8 MHz/DC[2]
Suspend	DC	9.2 MHz/DC[4]	14.3 MHz/DC[2]	4.6 MHz/DC[4]	DC	1.19 MHz/DC[2]	1.8 MHz/DC[2]
Off	DC	9.2 MHz/DC[4]	14.3 MHz/DC[3]	4.6 MHz/DC[4]	DC	1.19 MHz/DC[3]	1.8 MHz/DC[3]

Notes:

All power management features will be disabled when AC power is detected via the ACIN pin being High. A register is provided to implement "software ACIN" by writing 1 to bit 5 in the Switch 2 Register, Index 70H.

The DMA clock can be stopped except during DMA transfers. The Function Enable Register, Index B0H, controls this function.

The CPU clock speed in Low Speed mode is selectable, (see the Miscellaneous Control Register 3, Index ADH).

The CPU Clock speed:

1. *Can be programmed to run intermittently (on IRQ0) at 9.2 MHz.*
2. *Programmable option (but not on per-clock basis; i.e., all clocks with this note are controlled by a single ON/OFF select for that PMU mode).*
3. *Programmable option, will reflect setting in Suspend mode.*
4. *Can be programmed to run at 9.2 MHz during temporary-on NMI/SMI handlers.*

PMC and PGP Pins

The Am386SC300 microprocessor supports five power management control (PMC) pins and four programmable general purpose (PGP) pins. The PMC pins can be used to control the VCC rails of peripheral devices. The PMC pins are related to the operating modes of the Am386SC300 microprocessor PMU. The PGP pins can be used as general I/O chip selects for various uses.

The PMC4–PMC0 pins are controlled by Configuration Registers at Index 80H, 81H, ABH, and ACH. Basically, each pin can be programmed to be activated upon entry into any of the PMU modes or driven directly by software. So, PMC0 can be activated when the system is in High Speed PLL or Low Speed PLL modes; PMC1 when the system is in Doze mode; PMC2 when the system is in Sleep mode; PMC3 and PMC4 when the system is in Suspend mode; or just about any other combination. These pins can then be used by the system designer to shut off power to particular peripherals when the system enters certain modes, just as internal clocks are slowed or stopped in these modes. Upon the rising edge of $\overline{\text{RESIN}}$, PMC0, PMC1, PMC2, and PMC4 are asserted Low and PMC3 is asserted High. Prior to this edge, these signals are undefined.

The Am386SC300 microprocessor can be programmed to reset a timer when an I/O access to a preset address range is detected. If no I/O activity in that range occurs before the timer expires, the Am386SC300 microprocessor can assert a PMC signal to turn off the device. When S/W accesses that address range later, the Am386SC300 microprocessor can generate a System Management Interrupt (SMI) to the processor, which then activates an SMI handler routine. This routine then can determine the cause of the SMI and take appropriate action, such as powering the I/O device back on.

The PGP3–PGP0 pins are controlled by several configuration registers (70H, 74H, 89H, 91H, 94H, 95H, 9CH, A3H, and A4H) and their behavior is very flexible. PGP0 and PGP1 can be programmed as input or output. PGP2 and PGP3 are dedicated outputs. PGP1 and PGP3 can be gated with I/O reads, PGP0 and PGP2 can be gated with I/O writes, or each can act as an address decode for a chip select.

Micro Power Off Mode

The following paragraphs describe the Élan device in Micro Power Off mode. The following are distinctive characteristics:

- Minimum power consumption mode (approximately 25 µA typical, AVCC, and Core VCC combined).
- Allows the system designer to utilize the internal RTC and RTC RAM to maintain time, date, and system configuration data while the other system peripherals are powered off.
- Provides the system designer with the option of keeping the system DRAM powered and refreshed while other system peripherals are powered off. Self refresh and CAS-before-RAS refresh DRAMs are supported.
- Minimal external logic required to properly control power supplies and/or power switching.
- No external buffering required to properly power down system hardware.

The Élan device allows a system designer to easily maintain the internal RTC and RTC RAM and optionally, the DRAM interface, while the rest of the system peripherals attached directly to the device are powered off. All Am386SC300 power pins associated with the I/O pins of external powered off peripherals must be powered down also. This, in addition to internal Am386SC300 termination, provides the required isolation to allow the external peripherals to be powered off.

Automatically controlled internal I/O termination is provided to terminate the internal nodes of the Élan device properly when required.

The DRAM CAS-before-RAS, or self refresh, can be maintained by the Am386SC300 device in this Micro Power state, if configured to do so, utilizing the 32-kHz oscillator. This clock continues to drive the RTC and a portion of the core logic. The VMEM power plane (DRAM/SRAM section power) must remain powered on if the CAS-before-RAS refresh option is selected while in the Micro Power state. The VMEM power plane must also remain powered on if the self-refresh option is selected and the specific DRAM device requires any of its control pins (i.e., $\overline{\text{WE}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, etc.) to remain inactive in the Self-Refresh mode. If this is not required, it may be possible for the system designer to remove power from the VMEM pins when entering the Micro Power state, even if the Self-Refresh mode DRAMs remain powered on.

A portion of a typical system using a secondary power supply to maintain the RTC and RTC RAM (and optionally system DRAM) is shown in Figure 3. This secondary power supply could be as simple as a small lithium coin cell battery as indicated in the diagram, but is certainly not limited to this. Note that when all primary power supply outputs are turned off, all of the system's peripherals are powered off (DRAM optional), all of the Am386SC300 device's power planes are powered off except AVCC (analog) and VCC (core), and the secondary power supply is "switched in" to maintain the Am386SC300 device's core and analog power source.

The RESIN pin acts as the master reset. When active, all of the internal components are reset, including the RTC, and the RTC RAM invalid bit will be set. Therefore, the RESIN pin should only be asserted (pulsed) Low when a power source is initially applied to the device's core and analog sections. The IORESET signal is intended to be the normal "POWER GOOD" status from the primary power supply in this example design. The IORESET input does not reset the RTC and will not set the RTC RAM invalid bit.

IORESET (when the inactive state is detected) will cause the Am386SC300 device to go through its power up sequence including PLL start up for clock generation and an internal CPU reset. See Figures 31 through 34, beginning on page 90 for the initial power-up timing requirements, and for Micro Power mode exit timing.

When entering Micro Power mode and the primary power supply outputs are turned off, all of the Am386SC300 device's powered-down I/O pins are essentially 3-stated and the internal pullups are removed because the VCCIO and VCC CLAMP of the output driver have been removed, as shown in Figure 33 on page 91. This provides the ability to power off external peripherals that are attached directly to the Am386SC300 device without concern of the device driving current into the pins of the external powered-down device.

In order to assure that the Am386SC300 device does not draw excessive power while in this state, internal pull-down resistors will be enabled. Enabling these resistors keep the input buffers from floating (see Figure 4, Élan I/O Structure).

The Élan device samples the two reset inputs (RESIN and IORESET) to logically determine what state the power pins are in; and, in turn, controls the internal pull-down resistors. Note that in Micro Power mode, the IORESET input should be terminated with a pull-down resistor if not driven Low by an external device (see Table 17 for information about Internal I/O Pulldown States).

Micro Power DRAM Refresh

The system designer has the option to keep the system DRAM powered up and refreshed while the Am386SC300 device is in the Micro Power state. A configuration bit exists in the PMU section of the core logic to realize this feature, called the Micro Power Refresh Enabled bit. This bit is bit 2 of the configuration register at Index BAH. If this bit is cleared (default), the core logic associated with the DRAM refresh will be disabled when the Am386SC300 device is in the Micro Power state. If the bit is set, the core logic associated with the DRAM refresh will be enabled and functional while the Am386SC300 device is in its Micro Power state.

The type of Micro Power DRAM refresh performed (CAS-before-RAS, or self refresh) will be the same as that for which the part was configured before the IORESET pin sampled Low. If the micro power refresh feature is enabled for CAS-before-RAS refresh, the system designer should maintain power on the VMEM power pin of the Am386SC300 device and not remove power from the DRAM devices. If the micro power refresh feature is enabled for self refresh, the system designer may or may not be required to maintain power on the VMEM power pin of the Am386SC300 device, depending on the specific requirement of the DRAM device in Self-Refresh mode. Power should not be removed from the DRAM device itself in either case.

The Micro Power Refresh bit will always be cleared whenever the RESIN input is sampled Low. Therefore, when the core is initially powered up, the Micro Power DRAM refresh feature will be disabled. This bit is unaffected by the IORESET input. This bit will provide the system BIOS with a mechanism to determine whether or not the system DRAM data has been retained after a reset (IORESET) has occurred.

If Self-Refresh mode is selected and enabled for Micro Power mode, then when Micro Power mode is exited, the Am386SC300 device will properly force a CAS-before-RAS refresh cycle to cause the DRAMs to exit the Self-Refresh mode. The Am386SC300 device then transitions to the normal CAS-before-RAS refresh mode. This functionality is exactly the same as the Self-Refresh mode exit when the CPU Clock Stopped mode is exited. The Am386SC300 device is currently designed to only generate one CAS-before-RAS refresh cycle to force the DRAM to exit the Self-Refresh mode. This is also true for the Micro Power DRAM refresh feature.

The timing diagrams in Figures 33 and 34 show the sequence required to guarantee a proper transition into the Micro Power state. This sequence is especially critical when the DRAM refresh option is selected. Note that the power pins of the Am386SC300 device must be kept stable for some time after the IORESET input has gone active. "Stable" means that these power pins should remain at least at their VCC (min) value for the specified time indicated in Figure 33.

RESIN and IORESET

The Am386SC300 device has two reset inputs in order to support the Micro Power mode. These two inputs are RESIN and IORESET. If Micro Power mode is not to be used, the system designer should drive these two inputs from a common power-on reset source. Note that the RESIN signal is a 3.3-V only input and is not 5-V safe.

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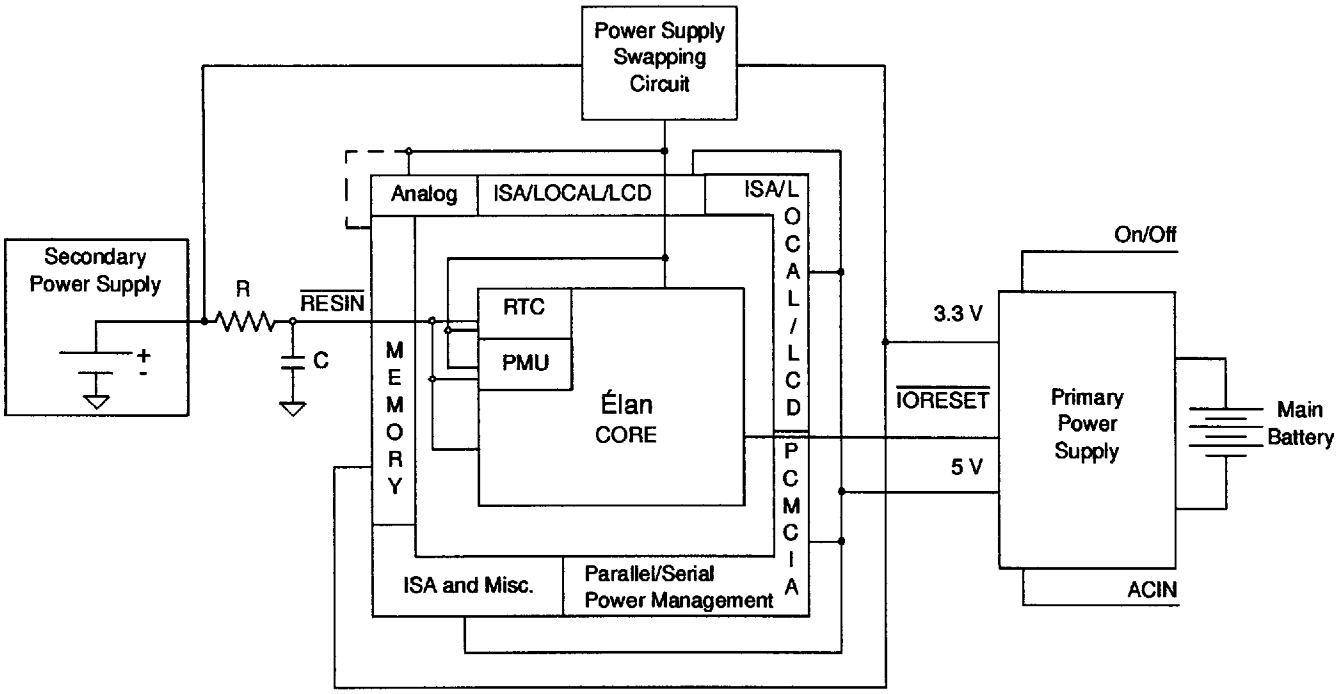


Figure 3. Typical System Design with Secondary Power Supply to Maintain RTC When Primary Power Supply Is Off. (DRAM Refresh Is Optional.)

Table 17. Internal I/O Pulldown States

$\overline{\text{IORESET}}$	$\overline{\text{RESIN}}$	Force Term	Comments
0	0	Active	This condition occurs when any power source is initially turned on. The Am386SC300 device's core and analog VCC is transitioning to on and $\overline{\text{RESIN}}$ is active (the initial power up state). See the Micro Power Off Mode Implementation section below for more details.
0	1	Active	This condition occurs when the core and analog VCC is stable, the $\overline{\text{RESIN}}$ pin has been inactive, and the primary power supply outputs are off (the normal Micro Power Off state).
1	0	Active	This condition should be treated as condition 0,0 above.
1	1	Inactive	This occurs when the secondary power supply is on, the $\overline{\text{RESIN}}$ input is inactive, and the primary power supply is on and has deasserted $\overline{\text{IORESET}}$ (normal system operating state).

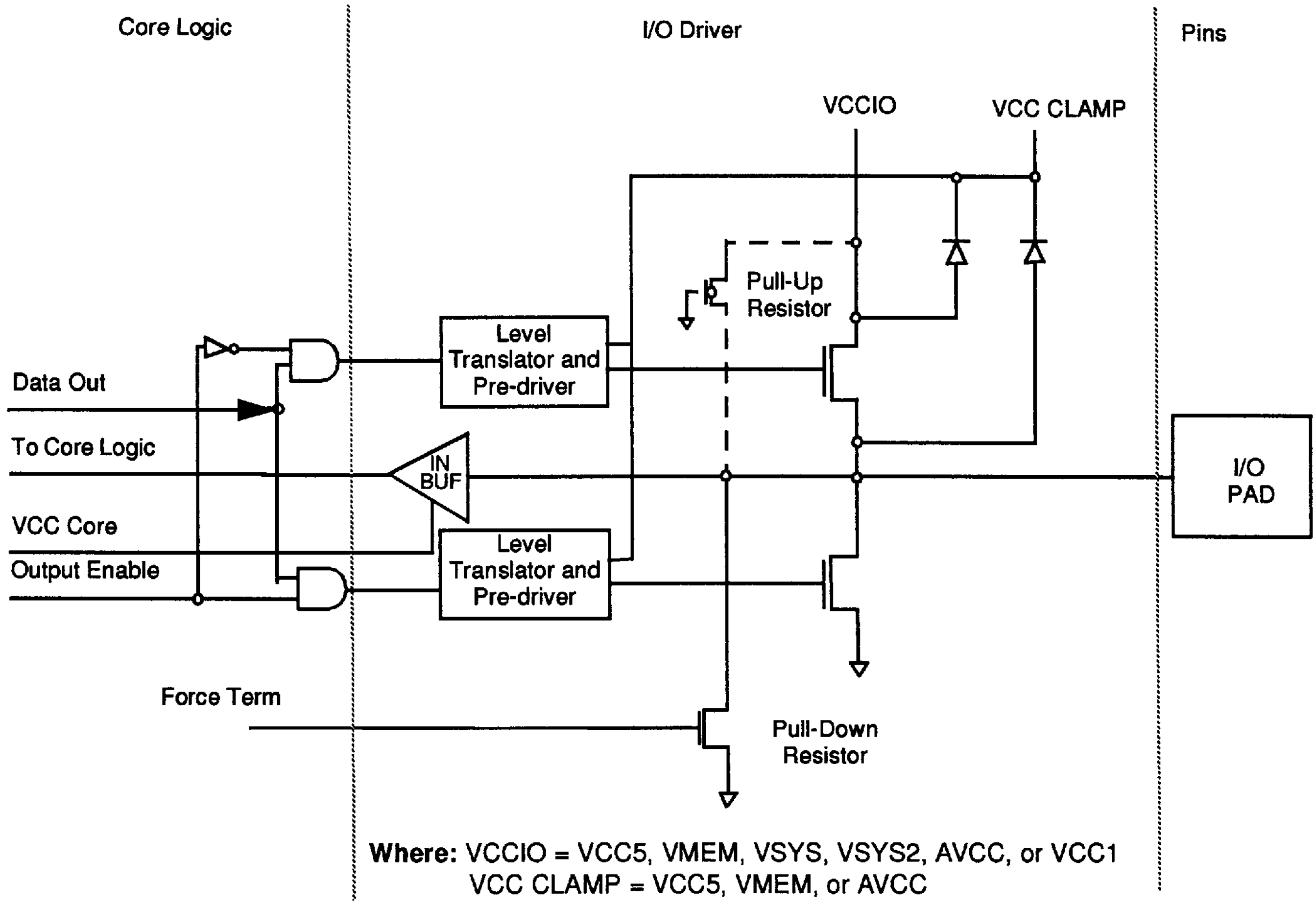


Figure 4. Élan I/O Structure

Micro Power Off Mode Implementation

A requirement for implementing Micro Power Off mode is to allow the system to come up fully on initial application of any power source. This insures that the Élan device is initialized properly before the initial transition into Micro Power Off mode.

This requirement presents an issue when using (for example) a 3-V Lithium battery cell as a backup power source to prevent the RTC from losing its contents during Micro Power Off mode. If the battery is installed before any other power source is available, the requirement cannot be met, since so small a battery is incapable of supplying sufficient power to fully initialize the system. The Élan device comes up in an undefined state, perhaps drawing sufficient current to drain the battery.

The Élan device backup power source should be installed only after the system is powered by the main power source prior to a transition into Micro Power Off mode. Once the system has transitioned into Micro Power Off mode properly, the simultaneous benefits of low power consumption while maintaining such RTC data as time, date, and system configuration can be realized.

Core Peripheral Controllers

The Am386SC300 microprocessor includes all the standard peripheral controllers that make up an AT system, including interrupt controller, DMA controller, counter-timer, and ISA bus controller.

Interrupt Controller

The Am386SC300 microprocessor interrupt controller is functionally compatible with the standard cascaded 8259A controller pair as implemented in the IBM PC AT.

The interrupt controller block accepts requests from peripherals, resolves priority on pending interrupts and interrupts in service, issues an interrupt request to the processor, and provides the interrupt vector to the processor.

The two devices are internally connected and must be programmed to operate in cascade mode for operation of all 15 interrupt channels. Interrupt controller 1 occupies I/O addresses 020H–021H and is configured for master operation in Cascade mode. Interrupt controller 2 occupies I/O addresses 0A0H–0A1H and is configured for slave operation.

The output of Timer 0 in the counter/timer section is connected to Channel 0 (IRQ0) of Interrupt controller 1. Interrupt request from the Real Time Clock is connected to Channel 0 (IRQ8) of Interrupt Controller 2. The other interrupts are available to external peripherals as in the AT architecture via the IRQ15–IRQ3 inputs. Other sources of interrupts are SMI/NMI and the PIRQ1–PIRQ0 inputs.

The Am386SC300 microprocessor interrupt controller has programmable sources for interrupts. These programmable sources are controlled by the configuration registers.

The Interrupt controller provides interrupt information to the Am386SC300 microprocessor power management unit to allow the monitoring of system activity. The Am386SC300 microprocessor power management unit can then use the interrupt activity to control the Power Management mode of the Am386SC300 microprocessor.

DMA Controller

The Am386SC300 microprocessor DMA controller is functionally compatible with the standard cascaded 8237 controller pair. Channels 0, 1, 2, and 3 are externally available 8-bit channels. DMA Channel 4 is the cascade channel. Channels 5, 6, and 7 are externally available as 16-bit channels.

Counter/Timer

The Élan device's counter/timer is functionally compatible with the 8254 device. A 3-channel general purpose 8254-compatible 16-bit counter/timer is integrated into the Am386SC300 microprocessor. It can be programmed to count in binary or in Binary Coded Decimal (BCD). Each counter operates independently of the other two and can be programmed for operation as a timer or a counter. All three are controlled from a common set of control logic, which provides controls to load, read, configure, and control each counter.

All of the 8254-compatible counter/timer channels are driven from a common clock, which is internally generated from the LS_PLL, 1.1892-MHz output. The output of Counter 0 is connected to IRQ0.

Additional Peripheral Controllers

The Am386SC300 microprocessor also integrates two other peripheral controllers commonly found in PCs, but not considered part of the "core peripherals," namely a serial port or a Universal Asynchronous Receiver Transmitter (UART), and a real-time clock (RTC).

16450 UART

The Am386SC300 microprocessor chip includes a UART, providing the Am386SC300 microprocessor systems with a serial port. This serial controller is fully compatible with the industry-standard 16450. In handheld systems, this port can connect to the pen input device or to a modem.

Real-Time Clock

The Am386SC300 microprocessor contains a fully 146818A-compatible Real-Time Clock (RTC) implemented in an AT-compatible fashion. The RTC drives its interrupt to power-management logic.

The RTC block in the Am386SC300 microprocessor consists of time of day clock with alarm and 100-year calendar. The clock/calendar can be represented in binary or BCD. It has a programmable periodic interrupt, and 128 bytes of static user RAM (an extension of the 146818A standard, see the programmer's reference manual for more details).

Parallel Port

The Am386SC300 microprocessor parallel port is functionally compatible with the PS/2 parallel port. The Am386SC300 microprocessor parallel port interface provides the parallel port control outputs and status inputs, and also the control signals for the parallel port data buffer/s. The parallel port data path is external to the Am386SC300 microprocessor. This interface can be configured to operate in either a unidirectional mode or bidirectional mode.

The unidirectional parallel port requires only one external component, the parallel port data latch. This latch is used to latch the data from the data bus and drive the data onto the parallel port data bus, as shown in Figure 5.

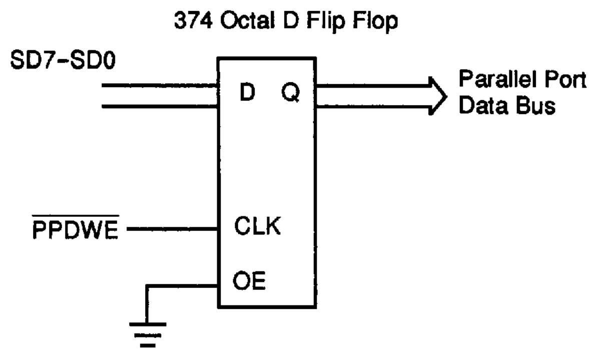


Figure 5. Am386SC300 CPU Unidirectional Parallel Port Data Bus Implementation

When the Am386SC300 microprocessor parallel port is configured for bidirectional mode operation, the $\overline{\text{PPDWE}}$ pin is reconfigured, via firmware, to function as the parallel port data register address decode ($\overline{\text{PPDCS}}$). The $\overline{\text{PPOEN}}$ output from the Am386SC300 microprocessor is controlled via the Parallel Port Control Register bit 5. This signal is then used to control the output enable of the external Parallel Port Data Latch. By setting this bit, the Parallel Port Data Latch is disabled, and then data can be transferred from an external Parallel Port device into the Am386SC300 microprocessor through an external 244-type buffer. A typical bidirectional Parallel Port Data Bus implementation is shown in Figure 6.

If the VCC5 supply pins are connected to a 5-V supply, then the Parallel Port control signals will be driven by 5-V outputs and can be connected directly to the parallel port connector. If VCC5 is connected to 3.3 V, the parallel port control signals should be translated to 5 V.

The Am386SC300 CPU also supports Enhanced Parallel Port (EPP) mode. The EPP mode pins are defined in Table 18.

Table 18. Parallel Port EPP Mode Pin Definition

Normal Mode	EPP Mode	Description
$\overline{\text{STRB}}$	$\overline{\text{WRITE}}$	EPP Write signal. This signal is driven active during writes to the EPP data or address register.
$\overline{\text{AFDT}}$	$\overline{\text{DSTRB}}$	EPP Data Strobe. This signal is driven active during reads or writes to the EPP data register.
$\overline{\text{SLCTIN}}$	$\overline{\text{ASTRB}}$	EPP Address Strobe. This signal is driven active during reads or writes to the EPP address register.
$\overline{\text{ACK}}$	INTR	EPP Interrupt. This signal is an input used by the EPP device to request service.
BUSY	$\overline{\text{WAIT}}$	EPP Wait. This signal is used to add wait states to the current cycle. It is similar to the ISA IOCHRDY signal.

In Normal mode, the outputs shown in Table 18 function as open-collector or open-drain outputs. In EPP mode, these outputs must function as standard CMOS outputs that are driven High and Low. Figure 6 shows the design that should be used to support EPP mode.

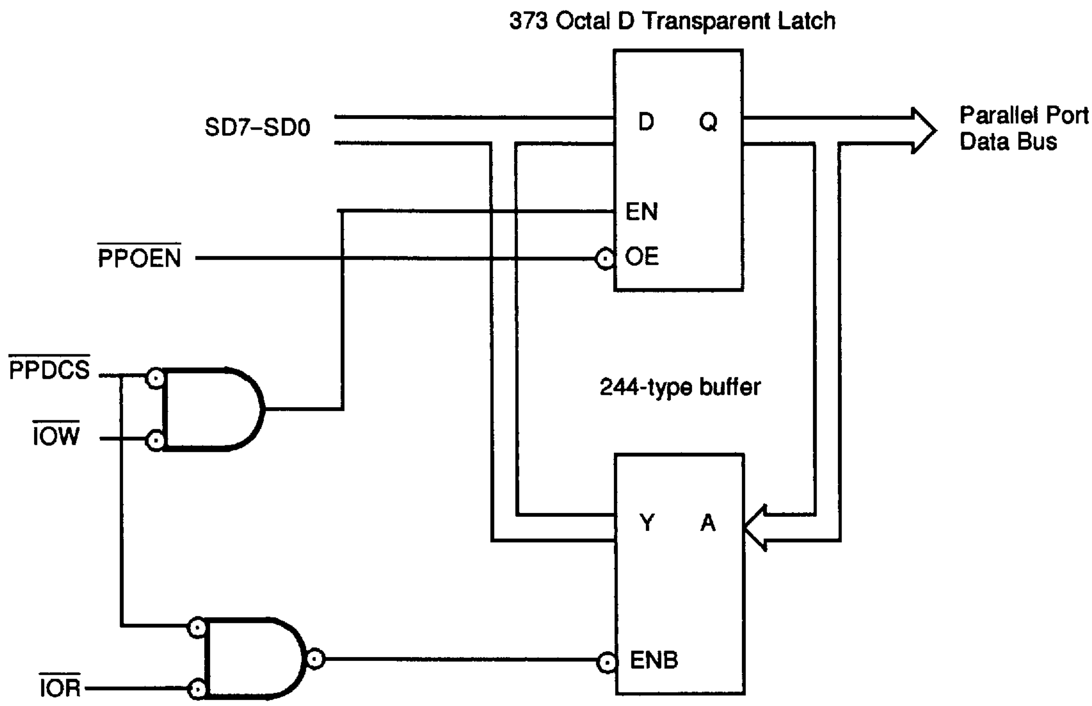


Figure 6. Am386SC300 CPU Bidirectional Parallel Port and EPP Implementation

Parallel Port Anomalies

General

The Am386SC300 microprocessor parallel port can be physically mapped to three different I/O locations or can be completely disabled. These I/O locations are 3BH, 37H, and 27H. Typically the system BIOS or a software driver sets up the port at system boot time. Generally, LPT1 is set up, by software, to be associated with IRQ7, and LPT2 (and LPT3, if desired) is setup to be associated with IRQ5. In the Am386SC300 microprocessor, the parallel port is always associated with IRQ7. This cannot be changed regardless of the I/O location to which the parallel port is mapped.

Local Bus or Maximum ISA Configuration

When the Am386SC300 microprocessor is configured for some bus mode other than the internal CGA controller option, the system BIOS should disable the internal video controller at boot time. This is done by setting bit 5 of the Screen Control Register 2, Index 19H in the CGA Index address space.

Control Register 1, Index 20H in the CGA index address space, controls the parallel port mapping. When the internal CGA controller is disabled, Control Register 1 cannot be accessed until the part is reset. Therefore, once the internal CGA controller has been disabled, the parallel port cannot be remapped. This can cause the system boot sequence to have to be modified such that the parallel port is set up prior to the disabling of the internal video controller. In addition, any software driver or setup utility, which was loaded after the internal video controller was disabled, would not have the ability to remap the parallel port location if this was required.

AT Support Features

The Am386SC300 microprocessor provides all of the support functions found in the original AT. These include the Port B status and control bits, speaker control, extensions for fast reset, and A20 gate control. (Fast CPU reset and fast A20 gate functions are controlled by either the Miscellaneous Register, Index 6FH, or Port 92H)

The Am386SC300 microprocessor also includes support for Port B, and a miscellaneous AT register that allows direct programming of the speaker via the SPK line. In addition, the Am386SC300 microprocessor also generates a chip select and clock source for an external, standard 8042 keyboard controller or the XT Keyboard feature.

Port B and NMI Control

Port B is an AT-standard miscellaneous feature control register that is located at I/O address 061H. The lower 4 bits of the 8-bit register are read/write control bits that enable or disable NMI check condition sources and sound generation features. The top, or most significant, 4 bits are read/write bits that return status and diagnostic information and control the XT Keyboard I/F.

There is a master NMI enable function provided that can inhibit any NMIs from reaching the CPU regardless of the state of the individual source enables. This master NMI control is located as a single bit (7) of the register at I/O address 070H. The default value for the NMI enable bit is 1, which inhibits NMI generation.The NMI enable bit (7) is a write-only bit, and is active Low. The remaining bits of the register located at 070H (6–0) control the RTC function. Because the RTC portion of this register is only 7 bits wide and is also write only, there is no conflict between the two functions. This register is discussed in more detail in the RTC section of Chapter 4 of the *Élan Am386SC300 Programmer's Reference Manual*, order #18470.

Speaker Interface

The AT standard tone generation interface for the system speaker is implemented in the Am386SC300 microprocessor. There are two data paths to the SPEAKER pin of the device. The first path is driven by the output of Channel 2 of the internal 82C54 counter/timer. The counter/timer can be programmed in various ways to generate a waveform at the output, OUT2. Also, the gate input of timer Channel 2 is controlled by the T2G bit in Port B. The timer gate can be used to inhibit tone generation by the timer channel. The second path is driven directly by the SPK bit in Port B. This bit can be manipulated by the CPU to generate almost any digital waveform at the SPEAKER pin.

Fast A20 Address Control

With the Am386SC300 microprocessor, full real mode address compatibility requires that address "rollover" at the 1-Mbyte address boundary be handled the same way the early 8088-based PCs were handled. This requires the system address line 20 to have the capability of being forced to a 0 during real mode execution. Control of the A20 line is supported from multiple sources.

The A20G signal in IBM PC/AT systems is normally connected to an output of the AT-keyboard controller. A logic High on this input forces the "pass through" of the CPU's A20 onto the internal system address bus. A logic Low on this input forces the system address bus A20 line Low, as long as the internal A20 gate control is not being utilized.

The Am386SC300 microprocessor provides a high performance method for controlling the system A20 line, independent of the relatively slow AT-keyboard controller. This internal A20 gate control is generated by the Miscellaneous Register, Index 6FH, and Port 92H.

Reset Control

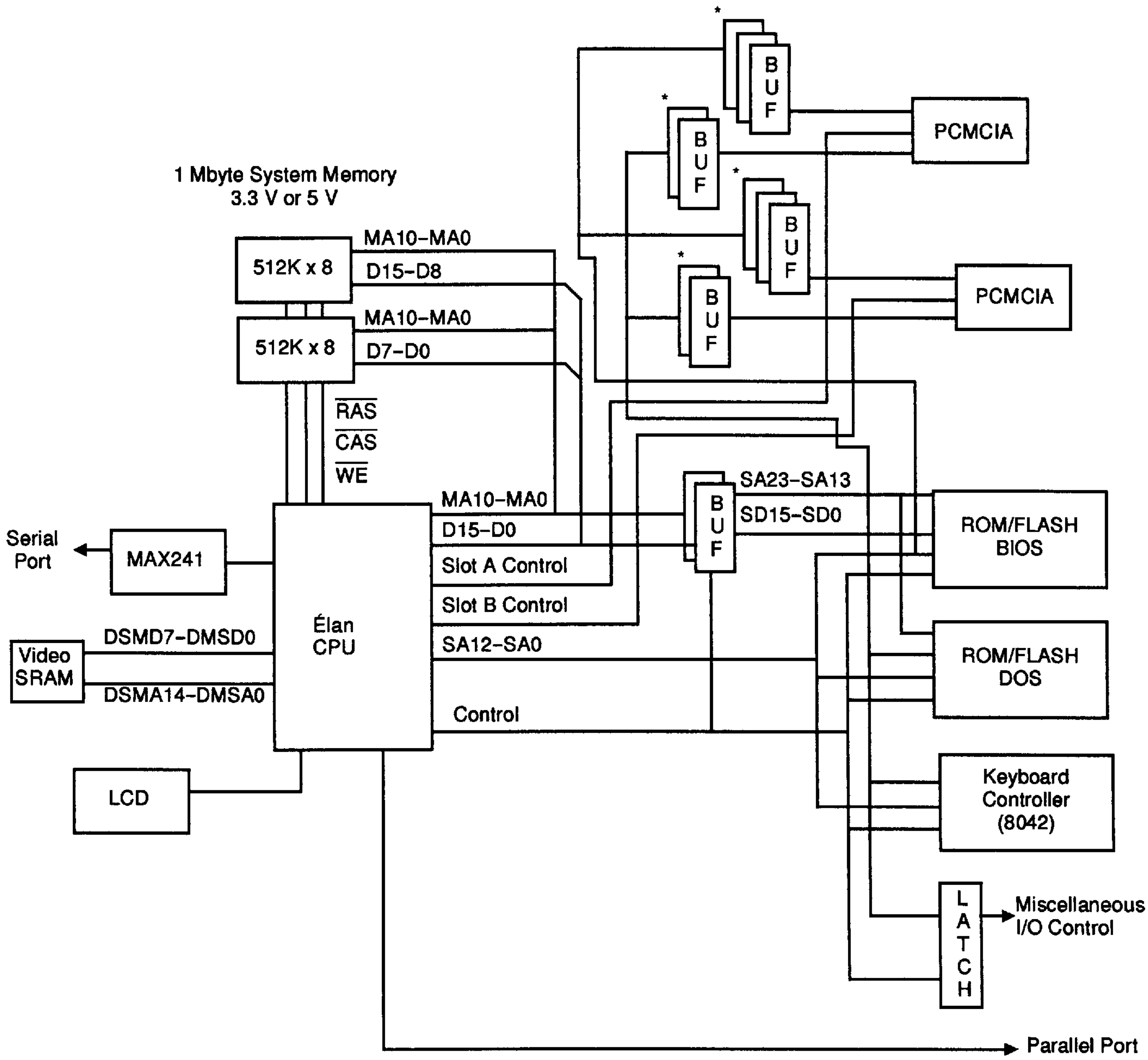
An external hardware reset is required in order to correctly initialize internal logic after system power-up. System power supplies typically have a POWERGOOD output signal that is used as an active Low asynchronous reset input for the device. $\overline{\text{IORESET}}$ is intended to be driven by a POWERGOOD-compatible signal. When $\overline{\text{IORESET}}$ is driven low, the Am386SC300 microprocessor resets all of its internal logic with the exception of the RTC Valid Data/Time bit (Register D,Index 0DH, bit 7) and some internal register configuration bits. The $\overline{\text{RESIN}}$ input is intended to be driven by a signal that indicates that the battery back-up source has not been disconnected. When $\overline{\text{RESIN}}$ is driven Low, the Am396SC300 microprocessor resets all of its internal logic. The $\overline{\text{RESIN}}$ input buffer is a Schmitt trigger, for tolerance of slow rise and fall times on the signal. $\overline{\text{RESIN}}$ and $\overline{\text{IORESET}}$ are internally synchronized to the CPU clock to provide the internal hardware reset.

Besides the device hardware reset, the internal CPU has several other possible reset sources. These other sources generate only CPU reset.

In a standard AT-type system, an $\overline{\text{RC}}$ (CPU Reset) pin is typically connected to an output of the 8042 keyboard controller.

Also, an internal configuration register can be used to reset the CPU in less time than that required by the external keyboard controller. The internal reset is controlled by the Miscellaneous Register, Index 6FH, and Port 92H.

The Am386SC300 microprocessor provides both of the Reset CPU functions described above and also triggers a CPU reset upon processor shutdown. If the CPU reaches a state where it cannot continue to execute because of faults and error conditions, it will issue a status code indicating shutdown, and the CPU will halt operation with no means of continuing except for a reset. If this shutdown status is detected, a 16-clock minimum pulse width reset is automatically sent to the CPU.



Note:
**Optional*

Figure 7. Typical System Block Diagram (Internal LCD Controller)

LCD, Local Bus, or Maximum ISA Bus Controller

Depending on the configuration chosen, the Am386SC300 microprocessor's pin functionality will differ. The three different options are Internal CGA Controller, Local Bus, and Maximum ISA Bus modes. The pin options are selected upon power-up reset. Only Internal CGA, Local Bus, or Maximum ISA Bus mode is available in a particular design. Both Internal CGA and Local bus do however provide a subset of the ISA bus.

The three sets of pin descriptions are described later in the section entitled Alternate Pin Functions.

Internal CGA Controller Option

The internal video controller is fully 6845 compatible, supporting up to 640 x 200 pixel LCD panels, or a CRT. This option supports an external 32-Kbyte SRAM for video memory. The smallest subset of ISA bus is available when using the internal CGA controller.

Local Bus Option

The local bus interface is integrated with the memory controller and the ISA bus controller, and it permits fast transfers to and from external local bus peripherals, such as video controllers. The local bus option is basically an Am386SXLV microprocessor local bus with an LDEV, LRDY, and CPUCLK added. Additional ISA bus signals are available in this mode.

Maximum ISA Bus Option

The Maximum ISA option provides the most ISA bus signals of any of the Am386SC300 microprocessor bus options. Since Master cycles and ISA refresh are not necessary in handheld designs, the Am386SC300 microprocessor does not provide these signals in any bus mode. The SYSCLK output from the Am386SC300 microprocessor is a clock that is normally only used for the external keyboard controller if one exists. This clock is 9.2 MHz and can be stopped completely.

This clock is not related to any of the ISA bus cycle timings. The ISA bus cycle timings vary depending on the clock speed selected for the internal ISA bus clock.

Table 19. External Resistor Requirements

Signal Name	Pin No.	Internal CGA		Local Bus		Maximum ISA		Notes
		Pull Up	Pull Down	Pull Up	Pull Down	Pull Up	Pull Down	
PIRQ0 (PIRQ0/IRQ3)	194	10K		10K		10K		
PIRQ1 (PIRQ1/IRQ6)	193	10K		10K		10K		
IRQ1	195	10K		10K		10K		
IOCHRDY	192	1K		1K		1K		
$\overline{\text{IOCS16}}$ [LCDDL0]	196	1K[-]		1K[-]		1K[-]		1
$\overline{\text{MCS16}}$ [LCDDL1]	197	1K[-]		1K[-]		1K[-]		1
IRQ14 [LCDDL2]	198	10K[-]		10K		10K		1
$\overline{\text{DTR}}$/CFG1	92		100K	10K			100K	2
$\overline{\text{RTS}}$/CFG0	93		10K		100K	10K		2
$\overline{\text{IORESET}}$	140		10K		10K		10K	
$\overline{\text{LVEE}}$ (IRQ15/IRQ15)	182			10K		10K		
M (IRQ4/IRQ4)	173			10K		10K		

Table 19. External Resistor Requirements (continued)

Signal Name	Pin No.	Internal CGA		Local Bus		Maximum ISA		Notes
		Pull Up	Pull Down	Pull Up	Pull Down	Pull Up	Pull Down	
LCDD2 [B] ($\overline{\text{IOCHCHK}}$/$\overline{\text{IOCHCHK}}$)	177			1K		1K		
$\overline{\text{DSWE}}$ ($\overline{\text{387ERR}}$/PULLUP)	183			100K		100K		
FRM [VDRV] (IRQ12/IRQ12)	181			10K		10K		
CP2 [VD0] ($\overline{\text{BUSY}}$/IRQ10)	179			1K		10K		
DSMA1 (PULLUP/IRQ7)	164			10K		10K		
DSMD0 ($\overline{\text{LDEV}}$/RESERVED)	148			1K				
LCDD3 [I] (DRQ1/ DRQ1)	174				10K		10K	3
LCDD1 [G] (DRQ5/ DRQ5)	175				10K		10K	3
CP1 [HDRV] (PREQ/ IRQ5)	178				10K	10K		
DSMD7 ($\overline{\text{ADS}}$/$\overline{\text{OWS}}$)	172					1K		
DSMD3 ($\overline{\text{BHE}}$/IRQ9)	168					10K		
DSMD2 ($\overline{\text{BLE}}$/IRQ11)	167					10K		
DSMA3 (CPUCLK/PULLUP)	162					1M		
DSMA0 (387RESET/PULLUP)	165					1M		
DSMD6 (D/$\overline{\text{C}}$ / DRQ0)	171						10K	3
DSMD5 (M/$\overline{\text{IO}}$ / DRQ3)	170						10K	3
DSMD4 (W/$\overline{\text{R}}$ / DRQ7)	169						10K	3
DSMD1 ($\overline{\text{LRDY}}$ / DRQ6)	166			1K			10K	3
DRQ2 [TDO]	76		10K		10K		10K	3
BVD2_A	113	10K		10K		10K		4
BVD1_A	114	10K		10K		10K		4
BVD2_B	119	10K		10K		10K		4
BVD1_B	120	10K		10K		10K		4
$\overline{\text{WAIT\_AB}}$	115	10K		10K		10K		4
$\overline{\text{CD\_A}}$	110	10K		10K		10K		4

Table 19. External Resistor Requirements (continued)

Signal Name	Pin No.	Internal CGA		Local Bus		Maximum ISA		Notes
		Pull Up	Pull Down	Pull Up	Pull Down	Pull Up	Pull Down	
$\overline{\text{CD\_B}}$	116	10K		10K		10K		4
RDY_A	111	10K		10K		10K		4
RDY_B	117	10K		10K		10K		4
WP_A	112	10K		10K		10K		
WP_B	118	10K		10K		10K		
$\overline{\text{DCD}}$	98	1M		1M		1M		
$\overline{\text{DSR}}$	97	1M		1M		1M		
$\overline{\text{SIN}}$	99	1M		1M		1M		
$\overline{\text{CTS}}$	96	1M		1M		1M		
$\overline{\text{RIN}}$	100	1M		1M		1M		
$\overline{\text{STRB}}$	83	4.7K		4.7K		4.7K		
$\overline{\text{AFDT}}$	80	4.7K		4.7K		4.7K		
$\overline{\text{INIT}}$	89	4.7K		4.7K		4.7K		
$\overline{\text{SLCTIN}}$	84	4.7K		4.7K		4.7K		
$\overline{\text{ERROR}}$	86	4.7K		4.7K		4.7K		
$\overline{\text{ACK}}$	88	4.7K		4.7K		4.7K		
BUSY	85	4.7K		4.7K		4.7K		
PE	82	4.7K		4.7K		4.7K		
SLCT	87	4.7K		4.7K		4.7K		
PGP0	189		100K		100K		100K	6
PGP1	188		100K		100K		100K	6
ACIN	101		10K		10K		10K	5
$\overline{\text{BL1}}$	106	100K		100K		100K		5
$\overline{\text{BL2}}$	107	100K		100K		100K		5
$\overline{\text{BL3}}$	108	100K		100K		100K		5

0257525 0048603 868

Table 19. External Resistor Requirements (continued)

Signal Name	Pin No.	Internal CGA		Local Bus		Maximum ISA		Notes
		Pull Up	Pull Down	Pull Up	Pull Down	Pull Up	Pull Down	
$\overline{BL4}$	109	100K		100K		100K		5
SOUT	94			10K				
RST_A	133		100K		100K		100K	
RST_B	127		100K		100K		100K	

***Notes:** All Pull Up and Pull Down resistor requirements are specified in ohms.*

1. *A [–] implies that for this "programmable" pin function, no external termination is required.*
2. *This pin is an "alternate pin function select input" that is sampled at reset. This pin functions as a normal serial port output after $\overline{RESIN}$ and $\overline{IORESET}$ are deasserted.*
3. *When this pin's function is a DMA request input, it should be terminated with a pull-down resistor if not connected to an external device that drives to a known state.*
4. *If this Am386SC300 microprocessor input is driven directly with a logic gate, then no external termination is required at the Am386SC300 microprocessor pin. The termination on the PCMCIA socket signal is still required per the PCMCIA 2.1 specification.*
5. *If this Am386SC300 microprocessor input is always driven to a known state, then no external termination is required.*
6. *If the pin is configured as an input, it should be terminated with a discrete pull-up or pull-down register, or it should always be driven to a known state.*

ALTERNATE PIN FUNCTIONS

To provide the system designer with the most flexibility, the Am386SC300 microprocessor provides a means for reconfiguring some of the pin functions, depending on the system requirements. Reconfiguration of the Am386SC300 microprocessor pin functions is accomplished in one of two ways, depending on the pin functions that are to be reconfigured. To select the internal LCD controller, CPU Local Bus Interface, or Maximum ISA Bus Interface, the state of the $\overline{\text{DTR}}$ and $\overline{\text{RTS}}$ pins are sampled on the rising edge of the $\overline{\text{RESIN}}$ and $\overline{\text{IORESET}}$ signals when power is first applied to the Am386SC300 microprocessor. This is shown in Figure 8 below.

After power has been initially applied and $\overline{\text{RESIN}}$ and $\overline{\text{IORESET}}$ are deasserted, additional assertions of $\overline{\text{IORESET}}$ while $\overline{\text{RESIN}}$ = 1 will not cause the pin configurations to change. However, the pin configuration inputs are always sampled in response to $\overline{\text{RESIN}}$ assertions. The following table shows the pin states at reset to enable the three different pin configurations involving the LCD controller, Local Bus, and Maximum ISA Bus. The bus configuration selected can be read in bits 5–7 of the Memory Configuration Register, Index 66H, after the reset.

Bus Option Select Bit Logic

Bus Selected	$\overline{\text{DTR}}$/CFG1	$\overline{\text{RTS}}$/CFG0
Internal LCD	0	0
Local Bus	1	0
Full / Maximum ISA	X	1

The second method of reconfiguring Am386SC300 device pin functions is accomplished by programming the internal configuration registers. This method is used to configure the following functions:

- DRAM or SRAM main memory interface
- Dual-scan LCD interface
- Unidirectional or bidirectional parallel port
- The clock source driving out on the X1OUT[BAUDOUT] pin
- External CRT monitor interface
- PCMCIA memory commands
- 14.336-MHz clock

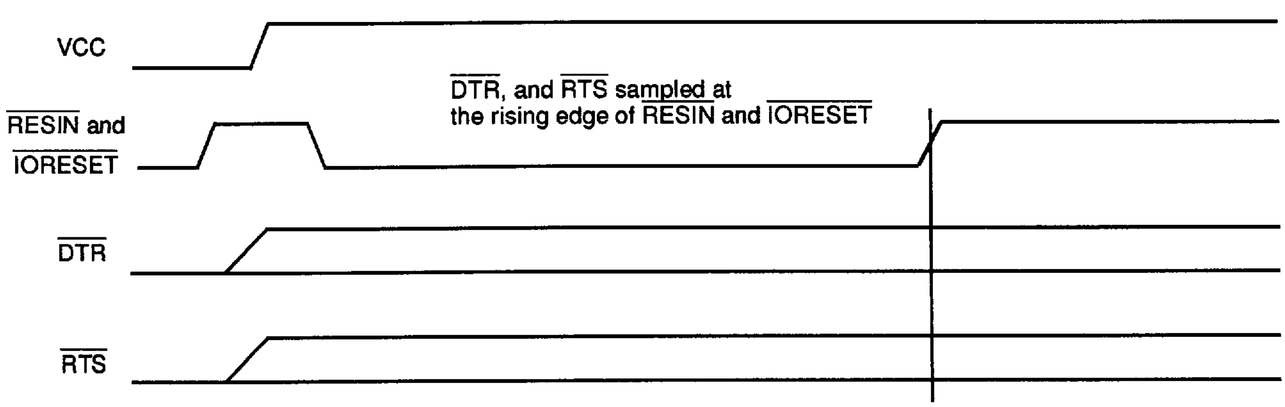


Figure 8. Bus Option Configuration Select

CPU Local Bus Interface

The tables of this section are brief descriptions of the alternate pin functions/names and the pin name of the Internal LCD mode function that the alternate function replaces. The CPU Local Bus Interface alternate functions are configured via the $\overline{DTR}$ and $\overline{RTS}$ pin states when the Am386SC300 microprocessor is reset.

Table 20. CPU Local Bus Interface Functions

CPU Local Bus Interface Pin Name	Pin Type	CPU Local Bus Interface Pin Description/Notes	Internal LCD Controller Mode Function Pin Name	Pin No.
A23–A12	O	Local Bus Address Bus	DSMA14–DSMA4 $\overline{LVDD}$	145 149–155 158–161
$\overline{ADS}$	O	Address Strobe	DSMD7	172
D/$\overline{C}$	O	Data/Code Cycle Status signal	DSMD6	171
M/$\overline{IO}$	O	Memory/I/O Cycle Status signal	DSMD5	170
W/$\overline{R}$	O	Write/Read Cycle Status signal	DSMD4	169
$\overline{BHE}$	O	Byte High Enable	DSMD3	168
$\overline{BLE}$	O	Byte Low Enable	DSMD2	167
$\overline{LRDY}$	I	Local Device Ready	DSMD1	166
$\overline{LDEV}$	I	Local Bus Device Acknowledge	DSMD0	148
$\overline{CPURDY}$	O	CPU Ready	$\overline{DSOE}$	147
CPUCLK	O	CPU Clock	DSMA3	162
387RESET	O	80387 Reset	DSMA0	165
PREQ	I	Processor Request	CP1[HDRV]	178
BUSY	I	Busy	CP2[VD0]	179
$\overline{387ERR}$	I	80387 Error	$\overline{DSWE}$	183
CPURST	O	CPU Reset	DSMA2	163

Notes:

1. *The SA11–SA0 pins are the lower order address lines for local bus cycles in the Local Bus Interface mode.*
2. *See the External Resistor Requirements section for information on required termination for Local Bus and Internal LCD Controller modes.*
3. *Other Internal LCD Controller mode pin functions, which are not listed in this table, change when the Local Bus mode is entered. These pins change to an ISA bus function when the Local Bus mode is entered.*

Maximum ISA Interface

The Maximum ISA Interface alternate functions are configured via the $\overline{\text{DTR}}$ and $\overline{\text{RTS}}$ pin states when the Am386SC300 microprocessor is reset.

Table 21. Maximum ISA Bus Interface Functions

ISA Interface Pin Name	Pin Type	ISA Interface Pin Description/Notes	Internal LCD Controller Mode Function Pin Name	Pin No.
$\overline{\text{IOCHCHK}}$	I	ISA I/O Channel Check input	LCDD2[B]	177
BALE	O	ISA Bus Address Latch Enable	$\overline{\text{LVDD}}$	145
DREQ0	I	DMA Channel 0 Request	DSMD6	171
DREQ1	I	DMA Channel 1 Request	LCDD3[I]	174
DREQ3	I	DMA Channel 3 Request	DSMD5	170
DREQ5	I	DMA Channel 5 Request	LCDD1[G]	175
DREQ6	I	DMA Channel 6 Request	DSMD1	166
DREQ7	I	DMA Channel 7 Request	DSMD4	169
$\overline{\text{DACK0}}$	O	DMA Channel 0 Acknowledge	DSMA7	158
$\overline{\text{DACK1}}$	O	DMA Channel 1 Acknowledge	$\overline{\text{DSCE}}$	146
$\overline{\text{DACK3}}$	O	DMA Channel 3 Acknowledge	DSMA6	159
$\overline{\text{DACK5}}$	O	DMA Channel 5 Acknowledge	LCDD0[R]	144
$\overline{\text{DACK6}}$	O	DMA Channel 6 Acknowledge	DSMA4	161
$\overline{\text{DACK7}}$	O	DMA Channel 7 Acknowledge	DSMA5	160
IRQ4	I	Interrupt Request input	M	173
IRQ5	I	Interrupt Request input	CP1[HDRV]	178
IRQ7	I	Interrupt Request input	DSMA1	164
IRQ9	I	Interrupt Request input	DSMD3	168
IRQ10	I	Interrupt Request input	CP2[VD0]	179
IRQ11	I	Interrupt Request input	DSMD2	167
IRQ12	I	Interrupt Request input	FRM[VDRV]	181
IRQ15	I	Interrupt Request input	$\overline{\text{LVEE}}$	182
LA23–LA17	O	ISA non-Latched Address bus	DSMA14–DSMA8	149–155
LMEG	O	ISA Memory Address Decode Below 1 Mbyte	$\overline{\text{DSOE}}$	147

Note:

See the External Resistor Requirements section for information on required termination for Maximum ISA Bus and Internal LCD Controller modes.

ALTERNATE PIN FUNCTIONS SELECTED VIA FIRMWARE

The following tables contain brief descriptions of the alternate pin functions/names and the pin names of the default function that the alternate function replaces. These alternate functions are selected via system firmware only.

SRAM Interface

This alternate function is configured by setting bit 0 of the Switch 2 Register, Index 70H.

Table 22. SRAM Interface

SRAM Pin Name	Pin Type	SRAM Interface Pin Description/Notes	Default Pin Name/Function	Pin No.
[$\overline{\text{SRCS0}}$]	O	SRAM Bank 0 Chip Select. Low Byte	$\overline{\text{CAS0L}}$	4
[$\overline{\text{SRCS1}}$]	O	SRAM Bank 0 Chip Select. High Byte	$\overline{\text{CAS0H}}$	5
[$\overline{\text{SRCS2}}$]	O	SRAM Bank 1 Chip Select. Low Byte	$\overline{\text{CAS1L}}$	6
[$\overline{\text{SRCS3}}$]	O	SRAM Bank 1 Chip Select. High Byte	$\overline{\text{CAS1H}}$	7

Dual-Scan LCD Data Bus

This alternate function is configured via selecting a dual-scan LCD Panel mode in the CGA index address space at Index 18H.

Table 23. Dual-Scan LCD Data Bus

Dual-Scan Pin Name	Pin Type	Dual-Scan LCD Data-Bus Pin Description/Notes	Default Pin Name/Function	Pin No.
[LCDDL0]	O	Dual Screen data bit	$\overline{\text{IOCS16}}$	196
[LCDDL1]	O	Dual Screen data bit	$\overline{\text{MCS16}}$	197
[LCDDL2]	O	Dual Screen data bit	IRQ14	198
[LCDDL3]	O	Dual Screen data bit	$\overline{\text{SBHE}}$	143

Note:

In this configuration, $\overline{\text{IOCS16}}$ and $\overline{\text{MCS16}}$ are internally forced inactive.

Unidirectional/Bidirectional Parallel Port

This alternate function is configured via selecting either the normal bidirectional mode configuration or the EPP mode configuration for the parallel port in the Function Enable Register, Index B0H.

Table 24. Bidirectional Parallel Port Pin Description

Bidirectional Pin Name	Pin Type	Bidirectional Parallel Port Pin Description/Notes	Default Pin Name/Function	Pin No.
[$\overline{\text{PPDCS}}$]	O	Parallel Port data register address decode	$\overline{\text{PPDWE}}$	90

X1OUT [BAUDOUT] Clock Source

The internal clock source driving out on this pin is configured via register bits of the Function Enable Registers, Index B0H and B1H.

Table 25. X1OUT Clock Source Pin Description

BAUDOUT Pin Name	Pin Type	X1OUT [BAUDOUT] Pin Description/Notes	Default Pin Name/Function	Pin No.
[BAUDOUT]	O	Serial baud rate clock	X1OUT	200

Note:
The default function of this pin is that no clock is driven out and the pin is 3-stated.

XT Keyboard

The XT Keyboard functionality is enabled via bit 4 of PMU Control Register 3, Index ADH.

Table 26. XT Keyboard Pin Description

XT Keyboard Pin Name	Pin Type	XT Keyboard Pin Description/Notes	Default Pin Name/Function	Pin No.
[XTDAT]	I/O	Keyboard data	$\overline{\text{8042CS}}$	75
[XTCLK]	I/O	Keyboard clock	SYSCLK	45

External CGA Monitor Interface

When the Am386SC300 microprocessor is configured for the internal LCD Controller mode, it can be configured to drive an LCD panel or a CGA monitor. These two displays cannot be driven simultaneously. The display type selection is configured via bit 4 of CGA Index register 18H.

Table 27. External CGA Monitor Interface

CGA Monitor Pin Name	Pin Type	CGA Monitor Pin Description/Notes	Default Pin Name/ Function	Pin No.
[R]	O	CGA compatible Red signal	LCDD0	144
[G]	O	CGA compatible Green signal	LCDD1	175
[B]	O	CGA compatible Blue signal	LCDD2	177
[I]	O	CGA compatible Intensity signal	LCDD3	174
[HDRV]	O	CRT horizontal synch	CP1	178
[VDO]	O	CRT dot clock	CP2	179
[VDRV]	O	CRT vertical synch	FRM	181

PCMCIA Data Path Control

Setting bit 4 of Miscellaneous Register 3, Index BAH, enables the PCMCIA memory commands on the Parallel port pins SLCTIN and INIT.

Table 28. PCMCIA Data Path Control

PCMCIA Control Pin Name	Pin Type	Data Path Control Pin Description/Notes	Default Pin Name/ Function	Pin No.
[$\overline{\text{PCMCOE}}$]	O	PCMCIA Output Enable	$\overline{\text{SLCTIN}}$	84
[$\overline{\text{PCMCWE}}$]	O	PCMCIA Write Enable	$\overline{\text{INIT}}$	89

14-MHz Clock Source

Setting bit 3 of Miscellaneous Register 3, Index BAH, enables the 14.336-MHz clock signal on the parallel port pin AFDT.

Table 29. 14-MHz Clock Source

14-MHz Pin Name	Pin Type	14-MHz Clock Pin Description/Notes	Default Pin Name/ Function	Pin No.
[X14OUT]	O	14.336-MHz Clock	$\overline{\text{AFDT}}$	80

ISA BUS DESCRIPTIONS

The three bus configuration options (Internal LCD controller, local bus, or maximum ISA bus) each support a somewhat different subset of the ISA bus standard. The internal LCD controller option supports the smallest ISA subset. It is defined in Table 30, below.

Table 30. Internal LCD Controller Bus Mode ISA Bus Functionality

Pin Name	I/O	Function
SA23–SA0	O	System Address Bus
D15–D0	B	System Data Bus
IOCHRDY	I	I/O Channel Ready
RSTDRV	O	System Reset
$\overline{MEMW}$	O	Memory Write
$\overline{MEMR}$	O	Memory Read
$\overline{IOW}$	O	I/O Write
$\overline{IOR}$	O	I/O Read
AEN	O	DMA Address Enable
TC	O	Terminal Count
SYSCLK	O	System Clock (ISA bus timing is not derived from this clock)
IRQ1	I	Interrupt IRQ1
PIRQ0	I	Programmable IRQX
PIRQ1	I	Programmable IRQX
$\overline{DACK2}$	O	DMA Channel 2 Acknowledge
DRQ2	I	DMA Channel 2 Request
$\overline{IOCS16}$	I	I/O device is 16 bits*
$\overline{MCS16}$	I	Memory device is 16 bits*
IRQ14	I	Interrupt Request Input*
$\overline{SBHE}$	O	Byte High Enable*
X1OUT [BAUDOUT]	O	Video Oscillator (14.336 MHz)/ Serial Port Output

Note:
** These ISA functions are available in this mode as long as the internal LCD controller is not configured for a dual-scan LCD panel in which case these pins would be used as additional data bits for the LCD panel. In Local Bus mode and Maximum ISA mode, the ISA function is always available.*

The Local Bus configuration supports a larger ISA subset. The additional pins supported are shown in Table 31. The Maximum ISA Bus configuration adds the pins found in Table 32.

The default value for the NMI enable bit is 1, which inhibits NMI generation.

Table 31. Local Bus Mode Additional ISA Bus Functionality

Pin Name	I/O	Function
IOCHCHK	I	ISA I/O Channel Check
DRQ1	I	DMA Channel 1 Request
$\overline{DACK1}$	O	DMA Channel 1 Acknowledge
DRQ5	I	DMA Channel 5 Request
$\overline{DACK5}$	O	DMA Channel 5 Acknowledge
IRQ4	I	Interrupt Request Input
IRQ12	I	Interrupt Request Input
IRQ15	I	Interrupt Request Input

Table 32. Maximum ISA Bus Mode Additional ISA Bus Functionality

Pin Name	I/O	Function
BALE	O	ISA Bus Address Latch Enable
DREQ0	I	DMA Channel 0 Request
DREQ3	I	DMA Channel 3 Request
DREQ6	I	DMA Channel 6 Request
DREQ7	I	DMA Channel 7 Request
$\overline{DACK0}$	O	DMA Channel 0 Acknowledge
$\overline{DACK3}$	O	DMA Channel 3 Acknowledge
$\overline{DACK6}$	O	DMA Channel 6 Acknowledge
$\overline{DACK7}$	O	DMA Channel 7 Acknowledge
IRQ7	I	Interrupt Request Input
IRQ9	I	Interrupt Request Input

Table 32. Maximum ISA Bus Mode Additional ISA Bus Functionality (Continued)

Pin Name	I/O	Function
IRQ11	I	Interrupt Request Input
$\overline{\text{0WS}}$	I	Zero Wait State Request
LA23–LA17	O	ISA Non-Latched Address
$\overline{\text{LMEG}}$	O	ISA Memory Cycle Below 100000H
IRQ5	I	Interrupt Request Input
IRQ10	I	Interrupt Request Input

System Test and Debug

The Am386SC300 microprocessor provides test and debug features compatible with the standard Test Access Port (TAP) and Boundary-Scan Architecture (JTAG).

The test and debug logic contains the following elements:

- Five extra pins—TDI, TMS, TCK, TDO, and $\overline{\text{TRST}}$ (JTAGEN). JTAGEN is dedicated; the other four are multiplexed.
- Test Access Port (TAP) controller, which decodes the inputs on the Test Mode Select (TMS) line to control test operations.
- Instruction Register (IR), which accepts instructions from the Test Data Input (TDI) pin. The instruction codes select the specific test or debug operation to be performed or the test data register to be accessed.
- Test Data Registers: Boundary Scan Register (BSR), Device Identification Register (DID), and Bypass Register (BPR).

Test Access Port (TAP) Controller

The TAP controller is a synchronous, finite state machine that controls the sequence of operations of the test logic. The TAP controller changes state in response to the rising edge of TCK and defaults to the test-logic-reset state at power-up. Reinitialization to the test-logic-reset state is accomplished by holding the TMS pin High for five TCK periods.

Instruction Register

The Instruction Register is a 4-bit register that allows instructions to be serially shifted into the device. The instruction determines either the test to execute or the data register to access, or both. The least significant bit is nearest the TDO output. When the TAP controller enters the capture-IR state, the instruction register is loaded with the default instruction Idecode. This is done to test for faults in the boundary scan connections at the board level.

Boundary Scan Register

The Boundary Scan Register is a serial shift register from TDI to TDO, consisting of all the boundary scan register bits in each I/O buffer.

Device Identification Register

The Device Identification Register is a 32-bit register that contains the AMD ID code for the Am386SC300 microprocessor: 195FA003H.

Bypass Register

The Bypass Register provides a path from TDI to TDO with one clock cycle latency. It helps to bypass a chip completely while testing boards containing many chips.

Test Access Port Instruction Set

The following instructions are supported:

- Sample/Preload. This instruction enables the sampling of the contents of the boundary scan registers as well as the serial loading of the boundary scan registers through TDI.
- Bypass. This instruction connects TDI and TDO through a 1-bit shift register, the Bypass Register.
- Extest. This instruction enables the parallel loading of the boundary scan registers. The device inputs are captured at the input boundary scan cell and the device outputs are captured at the output boundary scan cells.
- Idecode. This instruction connects the ID code register between TDI and TDO. The ID code register contains the fixed ID code value for the device.

JTAG Software

The Am386SC300 device design uses a noncombined bidirectional cell. The effects of this bidirectional cell are that during a sample/preload test for every bidirectional pad cell, an additional shift must be performed to load data in all the boundary cells. The total number of shifts required for the device it is 173.

The following table shows the relative position of all the Elan device's JTAG cells. Note that:

- The chain starts at PMC2 (pin 77) connected to TDI.
- The chain ends at 8042CS (pin 75) connected to TDO.
- The control cells are located within the chain, their relative position being indicated in the table.
- The MUXed signals (TCK, TDI, TDO, and TMS) are not part of the cell chain.
- Control cells are active Low.

Table 33. Boundary Scan (JTAG) Cells. Order and Type

Pin No.	Name	Cell Position	Cell Type	Notes
77	PMC2	1	output	
78	$\overline{\text{RC}}$	2	input	
79	A20GATE	3	input	
80	$\overline{\text{AFDT}}$	4	output	
82	PE	5	input	
83	$\overline{\text{STRB}}$	6	output	
84	$\overline{\text{SLCTIN}}$	7	output	
85	BUSY	8	input	
86	$\overline{\text{ERROR}}$	9	input	
87	SLCT	10	input	
88	$\overline{\text{ACK}}$	11	input	
89	$\overline{\text{INIT}}$	12	output	
90	$\overline{\text{PPDWE}}$	13	bidir	
91	$\overline{\text{PPOEN}}$	14	bidir	
92	$\overline{\text{DTR}}$	15	bidir	
93	$\overline{\text{RTS}}$	16	bidir	
94	SOUT	17	bidir	
96	$\overline{\text{CTS}}$	18	input	
97	$\overline{\text{DSR}}$	19	input	
98	$\overline{\text{DCD}}$	20	input	
99	SIN	21	input	
100	$\overline{\text{RIN}}$	22	input	
101	ACIN	23	input	
102	EXTSMI	24	input	
103	$\overline{\text{SUS/RES}}$	25	input	
*	*	26	control	Control cell for pins 106–155
106	$\overline{\text{BL1}}$	27	input	
107	$\overline{\text{BL2}}$	28	input	
108	$\overline{\text{BL3}}$	29	input	
109	$\overline{\text{BL4}}$	30	input	
110	$\overline{\text{CD\_A}}$	31	input	
111	RDY_A	32	input	

Table 33. Boundary Scan (JTAG) Cells. Order and Type (continued)

Pin No.	Name	Cell Position	Cell Type	Notes
112	WP_A	33	input	
113	BVD2_A	34	input	
114	BVD1_A	35	input	
115	WAIT_AB	36	input	
116	CD_B	37	input	
117	RDY_B	38	input	
118	WP_B	39	input	
119	BVD2_B	40	input	
120	BVD1_B	41	input	
122	ICDIR	42	output	
123	MCEL_B	43	output	
124	MCEH_B	44	output	
125	VPP_B	45	output	
126	REG_B	46	output	
127	RST_B	47	output	
129	MCEL_A	48	output	
130	MCEH_A	49	output	
131	VPPA	50	output	
132	REG_A	51	output	
133	RST_A	52	output	
134	CA24	53	output	
136	CA25	54	output	
137	PMC0	55	output	
138	PMC1	56	output	
139	SPKR	57	output	
140	IORESET	58	input	
141	RESIN	59	input	
143	SBHE	60	output	
144	DI_R	61	output	
145	LVDD	62	output	
146	DSCE	63	output	
147	DSOE	64	output	
148	DSMD0	65	bidir	

Table 33. Boundary Scan (JTAG) Cells. Order and Type (continued)

Pin No.	Name	Cell Position	Cell Type	Notes
149	DSMA14	66	output	
150	DSMA13	67	output	
151	DSMA12	68	output	
152	DSMA11	69	output	
153	DSMA10	70	output	
154	DSMA9	71	output	
155	DSMA8	72	output	
*	*	73	control	Control cell for pins 158–200
158	DSMA7	74	output	
159	DSMA6	75	output	
160	DSMA5	76	output	
161	DSMA4	77	output	
162	DSMA3	78	output	
163	DSMA2	79	output	
164	DSMA1	80	bidir	
165	DSMA0	81	output	
166	DSMD1	82	bidir	
167	DSMD2	83	bidir	
168	DSMD3	84	bidir	
169	DSMD4	85	bidir	
170	DSMD5	86	bidir	
171	DSMD6	87	bidir	
172	DSMD7	88	bidir	
173	M	89	bidir	
174	D0_I	90	bidir	
175	D2_G	91	bidir	
177	D3_B	92	bidir	
178	CP1_HDRV	93	bidir	
179	CP2_VDO	94	bidir	
181	FRM/VDRV	95	bidir	
182	$\overline{\text{LVEE}}$	96	bidir	
183	$\overline{\text{DSWE}}$	97	bidir	
184	PMC4	98	output	

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Table 33. Boundary Scan (JTAG) Cells. Order and Type (continued)

Pin No.	Name	Cell Position	Cell Type	Notes
185	PMC3	99	output	
186	PGP3	100	bidir	
187	PGP2	101	bidir	
188	PGP1	102	bidir	
189	PGP0	103	bidir	
190	$\overline{\text{LPH}}$	104	output	
191	IOCHRDY	105	input	
193	PIRQ(1)	106	input	
194	PIRQ(0)	107	input	
195	IRQ1	108	input	
196	$\overline{\text{IOCS16}}$	109	bidir	
197	$\overline{\text{MCS16}}$	110	bidir	
198	IRQ14	111	bidir	
200	CLK14_O	112	output	
*	*	113	control	Control cell for pins 2–51
2	$\overline{\text{RAS0}}$	114	output	
3	$\overline{\text{RAS1}}$	115	output	
4	$\overline{\text{CAS1L}}$	116	output	
5	$\overline{\text{CAS1H}}$	117	output	
6	$\overline{\text{CAS0L}}$	118	output	
7	$\overline{\text{CAS0H}}$	119	output	
8	$\overline{\text{MWE}}$	120	output	
10	MA10	121	output	
11	MA9	122	output	
13	MA8	123	output	
14	MA7	124	output	
15	MA6	125	output	
16	MA5	126	output	
17	MA4	127	output	
18	MA3	128	output	
19	MA2	129	output	
21	MA1	130	output	
24	MA0	131	output	

Table 33. Boundary Scan (JTAG) Cells. Order and Type (continued)

Pin No.	Name	Cell Position	Cell Type	Notes
25	D15	132	bidir	
26	D14	133	bidir	
27	D13	134	bidir	
28	D12	135	bidir	
29	D11	136	bidir	
30	D10	137	bidir	
31	D9	138	bidir	
32	D8	139	bidir	
34	D7	140	bidir	
36	D6	141	bidir	
37	D5	142	bidir	
38	D4	143	bidir	
39	D3	144	bidir	
40	D2	145	bidir	
41	D1	146	bidir	
42	D0	147	bidir	
43	DOSCS	148	output	
44	ROMCS	149	output	
45	SYSCLK	150	bidir	
46	DACK2		*	This pin becomes TCK when JTAGEN is High.
47	AEN		*	This pin becomes TDI when JTAGEN is High.
49	TC		*	This pin becomes TMS when JTAGEN is High.
50	ENDIRL	151	output	
51	ENDIRH	152	output	
*	*	153	control	Control cell for pins 54–103
54	IOR	154	output	
55	IOW	155	output	
56	MEMR	156	output	
57	MEMW	157	output	
58	RSTDRV	158	output	
59	DBUFOE	159	output	
60	SA12	160	output	
61	SA11	161	output	

Table 33. Boundary Scan (JTAG) Cells. Order and Type (continued)

Pin No.	Name	Cell Position	Cell Type	Notes
62	SA10	162	output	
63	SA9	163	output	
64	SA8	164	output	
66	SA7	165	output	
67	SA6	166	output	
69	SA5	167	output	
70	SA4	168	output	
71	SA3	169	output	
72	SA2	170	output	
73	SA1	171	output	
74	SA0	172	output	
75	$\overline{\text{8042CS}}$	173	bidir	
76	DRQ2		*	This pin becomes TDO when JTAGEN is High.

JTAG Instruction Opcodes

The following table lists the Élan device's "public" JTAG instruction opcodes. Note that the JTAG Instruction Register is 4-bits wide.

Instruction	Opcode
EXTEST	0000
BYPASS	1111
SAMPLE/PRELOAD	0001
IDCODE	0010

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C

Ambient Temperature Under Bias ... −65°C to +125°C

Supply Voltage V_{CC} with
Respect to V_{SS} .... −0.5 V to +7 V

Voltage on Other Pins .... −0.5 V to (V_{CC}+0.5 V)

Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

DC CHARACTERISTICS over COMMERCIAL operating ranges (PQFP, 33 MHZ)

VCCIO = 3.0 V - 3.6 V; $T_{AMBIENT}$ = 0°C to +70°C

Symbol	Parameter Description	Preliminary			Unit
		Min	Typ	Max	
f_{osc}	Frequency of Operation (internal CPU clock)	0		33	MHz
P_{CC} (2)	Supply Power—CPU clock = 33 MHz (VCCMEM=3.3 V)		582	778	mW
P_{CCSS} (2)	Suspend Power—CPU idle, all internal clocks stopped except 32.768 kHz		0.12		mW
$V_{OH(CMOS)}$	Output High Voltage $I_{OH(CMOS)}$ = −0.5 mA	VCC-0.45			V
$V_{OL(CMOS)}$	Output Low Voltage $I_{OL(CMOS)}$ = 0.5 mA			0.45	V
$V_{IH(CMOS)}$	Input High Voltage	2.0		VCC+0.3	V
$V_{IL(CMOS)}$	Input Low Voltage	-0.3		+0.8	V
I_{LI}	Input Leakage Current (0.1 V≤V_{OUT}≤VCC) (all pins except those with internal pull-up/pull-down resistors)			±10	µA
I_{IH}	Input Leakage Current V_{IH} = VCC − 0.1 V (all pins with internal pull-down resistors)			60	µA
I_{IL}	Input Leakage Current V_{IL} = 0.1 V (pins with internal pull-up resistors)			-60	µA
I_{LO}	Output Leakage Current (0.1 V≤V_{OUT}≤VCC)			±15	µA
C_{in} (3)	I/O Capacitance			15	pF
$AVCC_{RP-P}$	Analog V_{CC} ripple peak to peak			100	mV

Notes:

1. *Current out of a pin is given as a negative value.*
2. *VCC, VCC1, AVCC = 3.3 V and VCC5, VCCSYS, VCCSYS2 = 5.0 V.*
3. *Fc = 1 MHz.*

DC CHARACTERISTICS over COMMERCIAL operating ranges (PQFP, 33 MHZ)

VCCIO = 4.5 V – 5.5 V; $T_{AMBIENT}$ = 0°C to +70°C

Symbol	Parameter Description		Preliminary Min	Preliminary Typ	Preliminary Max	Unit
f_{osc}	Frequency of Operation (internal CPU clock)		0		33	MHz
P_{CC} (2)	Supply Power—CPU clock = 33 MHz (VCCMEM=5 V)			660	862	mW
P_{CCSB} (2)	Suspend Power—CPU idle, all internal clocks stopped except 32.768 kHz			0.17		mW
$V_{OH(CMOS)}$	Output High Voltage	$I_{OH(CMOS)} = -0.5$ mA	VCC–0.45			V
$V_{OL(CMOS)}$	Output Low Voltage	$I_{OL(CMOS)} = 0.5$ mA			0.45	V
$V_{IH(CMOS)}$	Input High Voltage		2.0		VCC+0.3	V
$V_{IL(CMOS)}$	Input Low Voltage		–0.3		+0.8	V
I_{LI}	Input Leakage Current (all pins except those with internal pull-up/pull-down resistors)	$(0.1 - V \leq V_{OUT} \leq VCC)$			±10	µA
I_{IH}	Input Leakage Current (all pins with internal pull-down resistors)	$V_{IH} = VCC - 0.1$ V			90	µA
I_{IL}	Input Leakage Current (pins with internal pull-up resistors)	$V_{IL} = 0.1$ V			–90	µA
I_{LO}	Output Leakage Current	$(0.1 - V \leq V_{OUT} \leq VCC)$			±15	µA
C_{in} (3)	I/O Capacitance				15	pF
$AVCC_{RP-P}$	Analog VCC ripple peak to peak				100	mV

Notes:

1. *Current out of pin is given as a negative value.*
2. *VCC, VCC1, AVCC = 3.3 V and VCC5, VCCSYS, VCCSYS2 = 5 V.*
3. *Fc = 1 MHz.*

TYPICAL POWER NUMBERS

The tables below show the typical power numbers that were measured for the Am386SC300 microprocessor. These measurements reflect the part when it is configured for Maximum ISA and Internal CGA modes of operation at operating speeds of 33 MHz, 25 MHz, and 9.2 MHz. The connection of the various power sections of the part are outlined in the tables so that the designer may have some relative information for the power consumption differences between 3.3-V operation and 5-V operation. Please see the notes associated with the tables for specifics on the test conditions.

Typical Maximum ISA Mode Power Consumption

Power Pin			Maximum ISA Mode					
Group	Name	Volts	33 MHz	25 MHz	9.2 MHz	Doze[2]	Suspend[3]	μ Pwr Off[4]
CPU Core	VCC	3.3	119 mA	94.3mA	39.1mA	6.12 mA	5.7 μA	4.1 μA
I/O VCC	VCC1	5	5.55 mA	5.55mA	5.55mA	5.55 mA	0 μA	OFF
Analog	AVCC	3.3	2.58 mA	2.36 mA	2.24 mA	1.39 mA	19.9 μA	19.8 μA
I/O	VCC5	5	772 μA	680 μA	434 μA	293 μA	0 μA	OFF
Memory	VCCMEM	3.3	16.4 mA	12.6 mA	4.9 mA	190 μA	10.5 μA	OFF
Sub ISA Bus	VCCSYS	5	16.8 mA	13.7 mA	7.76 mA	3.6 mA	0 μA	OFF
Full ISA Bus	VCCSYS2	5	2.06 mA	1.57 mA	0.9 mA	21 μA	0 μA	OFF
Total (mW)			582 mW	468mW	226mW	72.7 mW	0.12 mW	0.08 mW

Memory[5]	VCCMEM	5	26.5 mA	20.3 mA	8.75 mA	304 μA	17 μA	OFF
Total (mW)			660 mW	528 mW	470 mW	73.6 mW	0.17 mW	0.08 mW

Typical Internal CGA Mode Power Consumption

Power Pin			Internal CGA Mode					
Group	Name	Volts	33 MHz	25 MHz	9.2 MHz	Doze[2]	Suspend[3]	μ Pwr Off[4]
CPU Core	VCC	3.3	121 mA	95.2 mA	40.1 mA	6.24 mA	5.5 μA	4.1 μA
I/O VCC	VCC1	5	14.8 mA	14.8 mA	14.8 mA	14.7 mA	0 μA	OFF
Analog	AVCC	3.3	2.62 mA	2.4 mA	2.24 mA	1.4 mA	19.9 μA	19.8 μA
I/O	VCC5	5	867 μA	765 μA	562 μA	448 μA	0 μA	OFF
Memory	VCCMEM	3.3	17 mA	13 mA	4.9 mA	182 μA	11.3 μA	OFF
Sub ISA Bus	VCCSYS	5	18.9 mA	15.3 mA	8.1 mA	3.85 mA	0 μA	OFF
Full ISA Bus	VCCSYS2	5	3.88 mA	3.86 mA	3.82 mA	3.79 mA	0 μA	OFF
Total (mW)			656 mW	539 mW	292 mW	140 mW	0.12 mW	0.08 mW

Memory [5]	VCCMEM	5	26.8 mA	20.4 mA	7.6 mA	300 μA	17.6 μA	OFF
Total (mW)			734 mW	598 mW	314 mW	141 mW	0.17 mW	0.08 mW

Notes:

All measurements were obtained at typical room temperature (ambient).

1. *In normal operating mode measurements, the Am386SC300 microprocessor is running the LandMark Speedcom benchmark (Version 2.00). All CPU idle cycles are run at the high speed rate.*
2. *In Doze mode, the Doze mode configuration is such that the low-speed CPU clock is programmed to turn on for 64 refresh cycles upon an IRQ0 (DOS timer) generation. After 64 refresh cycles, the low-speed CPU clock is turned off again. The IRQ0 timer is set for an approximate 55-ms interval and the refresh duty cycle is approximately 15.6 µs. In Doze mode, the high-speed PLL is always turned off and, in this case, the low-speed PLL and video PLLs are on to allow the IRQ0 periodic wake-up.*
3. *Suspend-mode measurements were taken with DRAM refresh rate set at 8192 Hz (126 µs).*
4. *Micropower measurements were taken with DRAM unpowered, and the DRAM refresh rate set at 8192 Hz.*
5. *These measurements were taken with the memory interface powered at 5 V, rather than 3.3 V.*

Table 34. I/O Drive Type Description (Worst-Case)

T_A= 70°C, $V_{OL_{TTL}}$ = 0.4 V, $V_{OH_{TTL}}$ = 2.4 V

I/O Drive Type	VCCIO (V)	IOL_{TTL} (mA)	IOH_{TTL} (mA)*
A	3.0 4.5	2.6 3.7	-3.5 -13.9
B	3.0 4.5	5.1 7.3	-5.2 -20.7
C	3.0 4.5	7.7 10.8	-8.6 -34.2
D	3.0 4.5	7.7 10.8	-10.3 -40.8
E	3.0 4.5	10.2 14.1	-13.6 -53.9

Note:

**Current out of pin is given as a negative value.*

DERATING CURVES

This section describes how to use the derating curves on the following pages in order to determine potential-specified timing variations based on system capacitive loading. The pin characteristics tables in this document (see page 12) have a column called "Spec. Load." This column describes the specification load presented to the specific pin when testing was performed to generate the timing specification documented in the "AC Characteristics" section of this document.

For example, to find out the effect of capacitive loading on a DRAM spec, such as MWE hold from CAS Low, first find the spec. load for MWE from the pin characteristics table. The value here is 70 pF. Note the output drive type is D. Also, assume that the system DRAM interface is 3.3 V and our system load on the Am386SC300 MWE pin is 90 pF.

Referring to Figure 13, 3.3-V I/O Drive Type D Rise Time, a time value of approximately 9.8 ns corresponds to a capacitive load of 70 pF.

Also referring to Figure 13, a time value of approximately 12.3 ns corresponds to a capacitive load of 90 pF. Subtracting 9.8 ns from the 12.3 ns, it can be seen that the rise time on the MWE signal will increase by 2.5 ns. Therefore, the MWE hold from CAS Low (Min) parameter will increase from 15 ns to (15 ns + 2.5 ns) = 17.5 ns.

If the capacitive load on MWE was less than 70 pF, the time given in the derating curve for the load would be subtracted from the time given for the specification load. This difference can then be subtracted from the MWE hold from CAS Low (min) parameter (ISNS) to determine the derated AC Timing parameter.

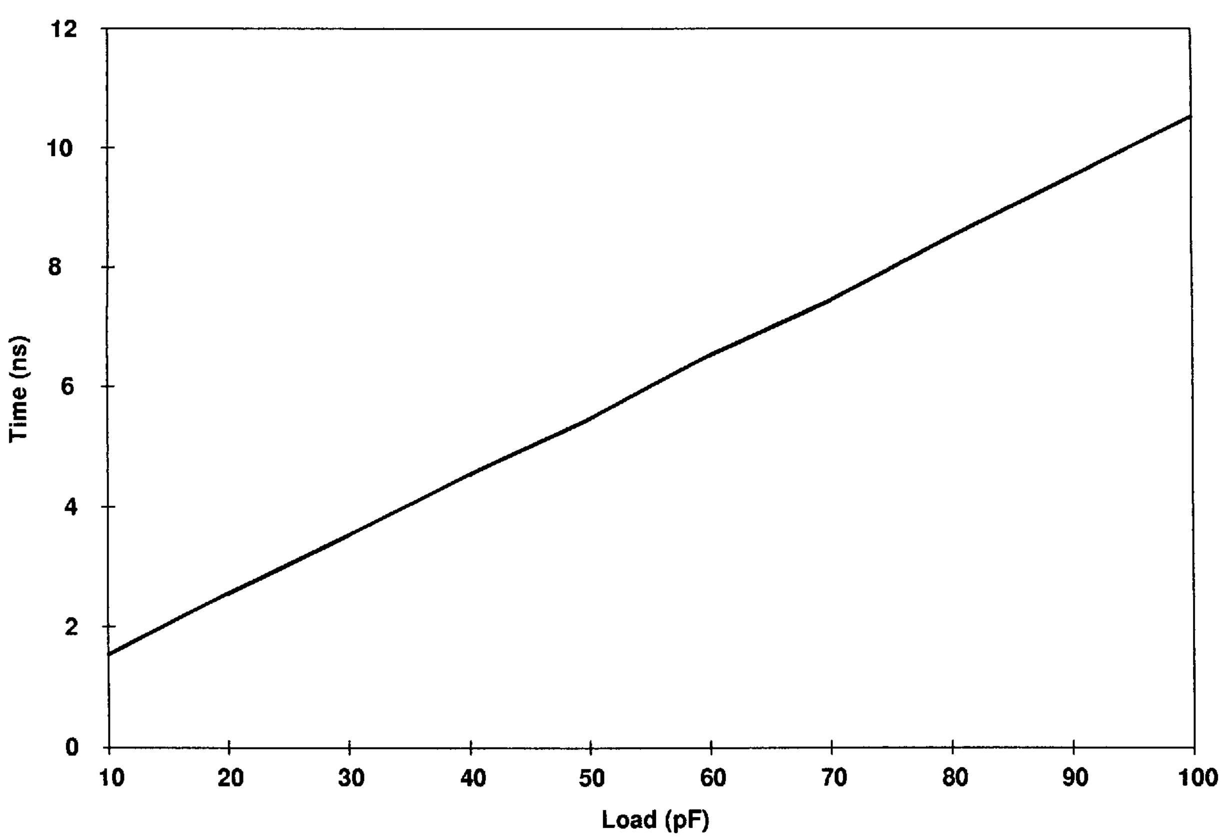


Figure 9. 3.3-V I/O Drive Type E Rise Time

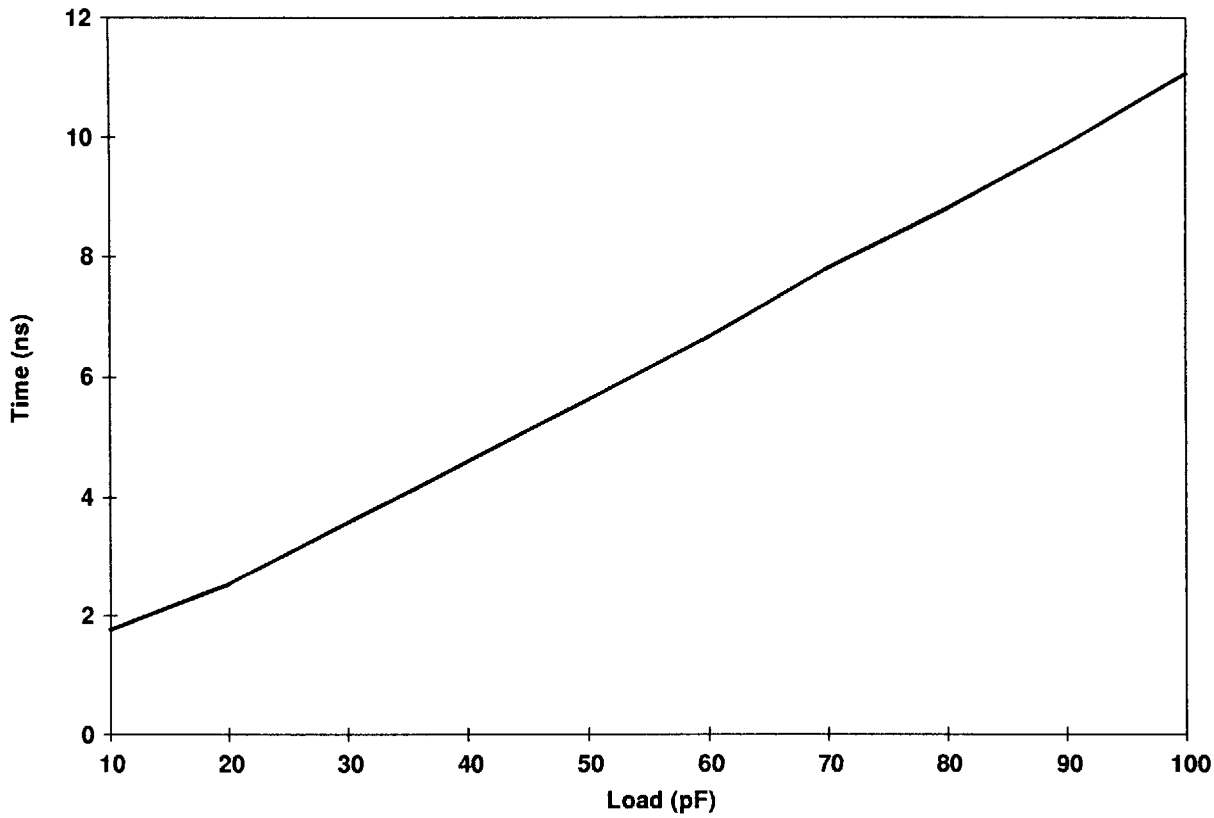


Figure 10. 3.3-V I/O Drive Type E Fall Time

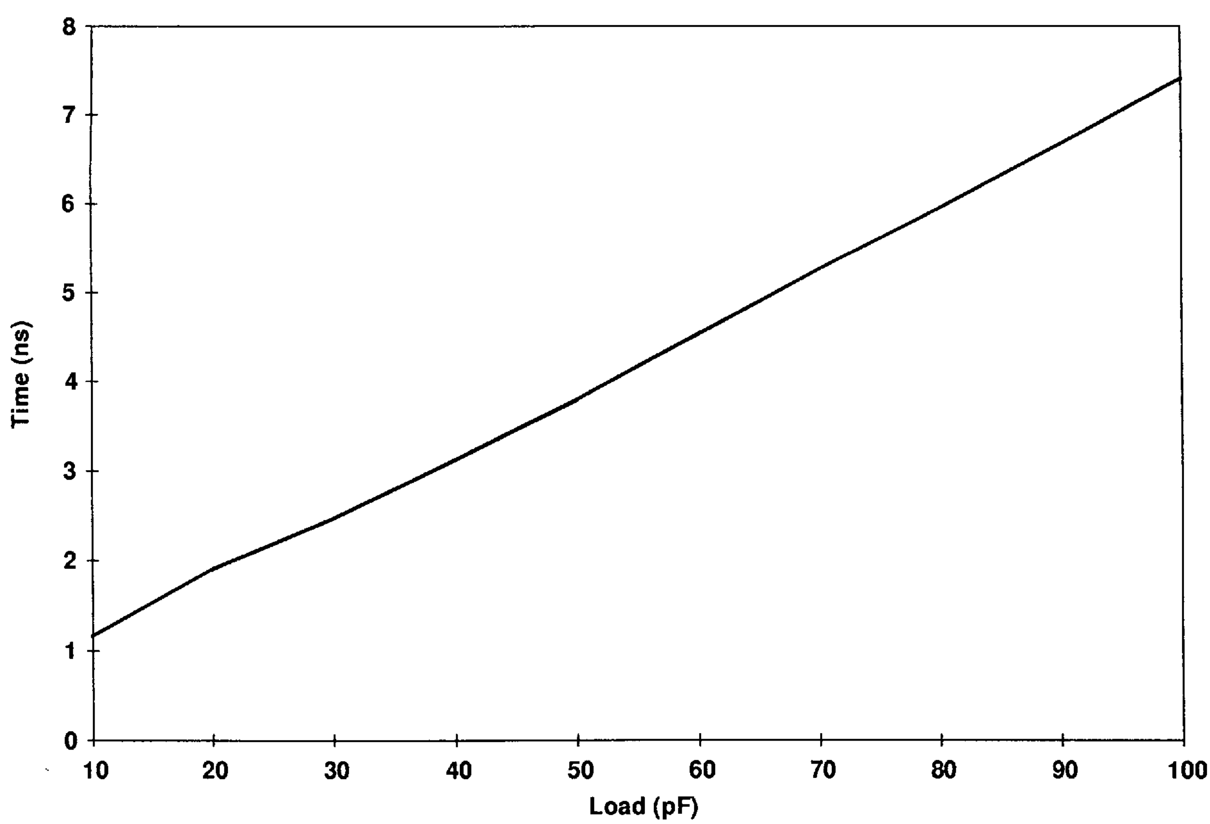


Figure 11. 5-V I/O Drive Type E Rise Time

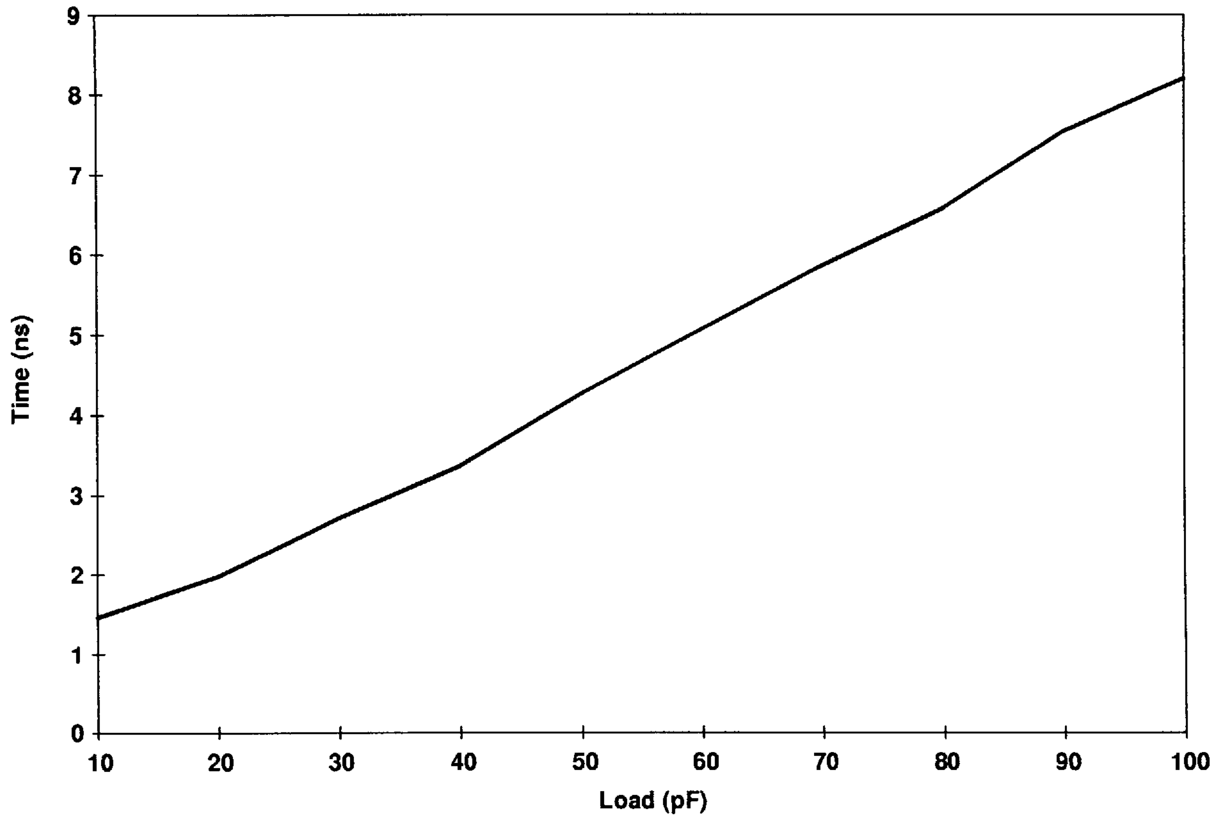


Figure 12. 5-V I/O Drive Type E Fall Time

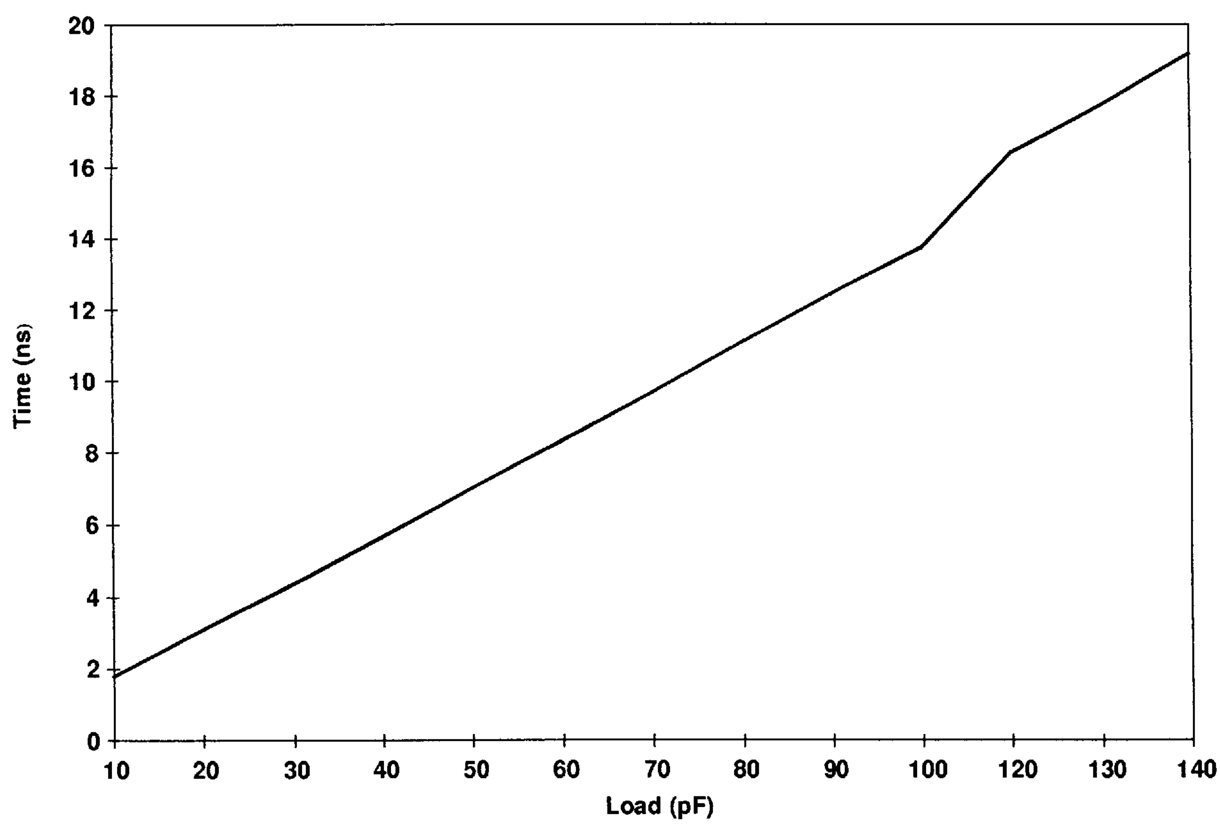


Figure 13. 3.3-V I/O Drive Type D Rise Time

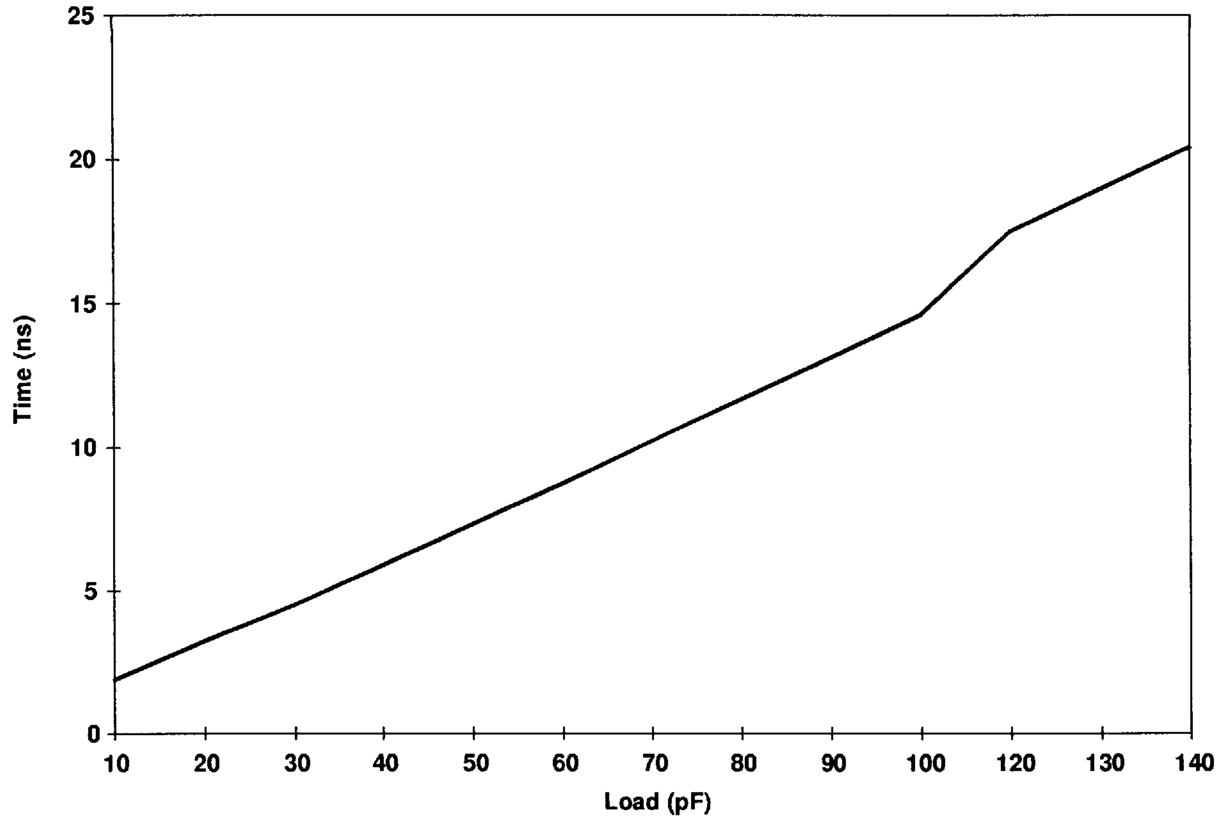


Figure 14. 3.3-V I/O Drive Type D Fall Time

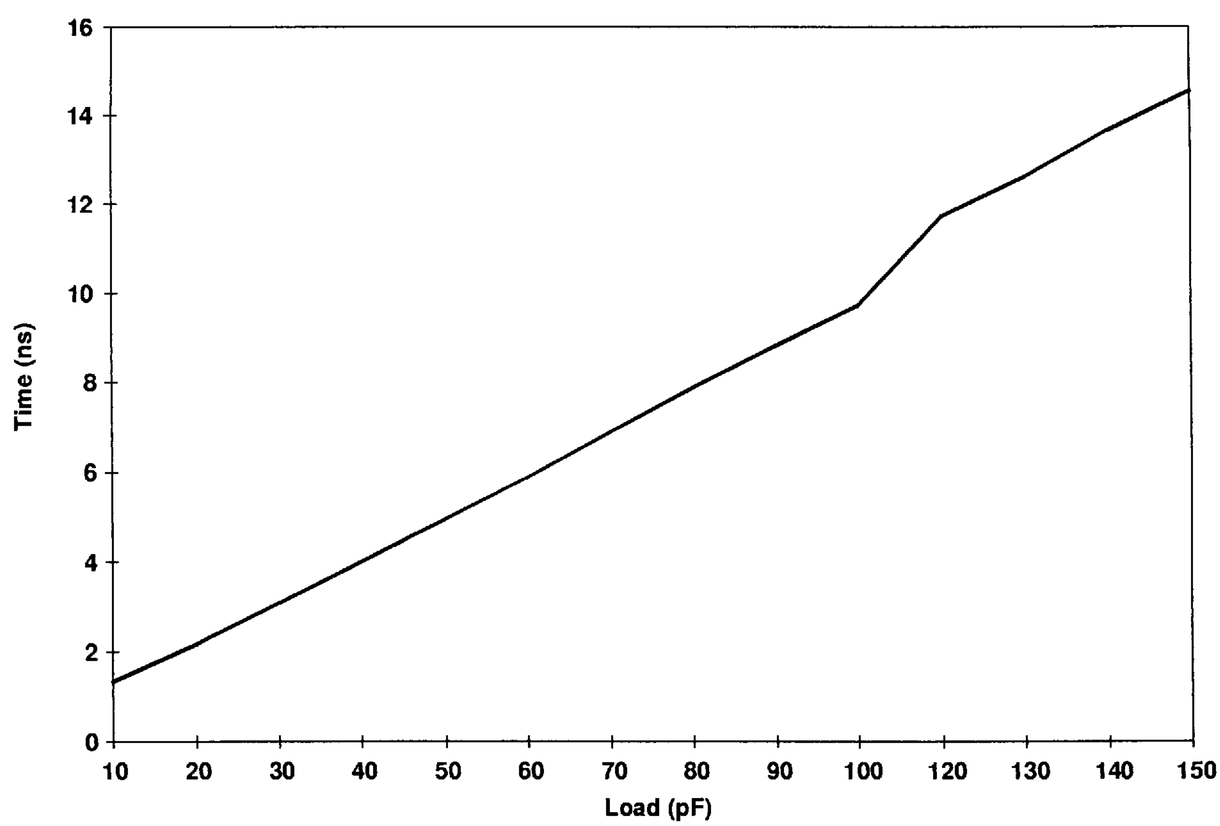


Figure 15. 5-V I/O Drive Type D Rise Time

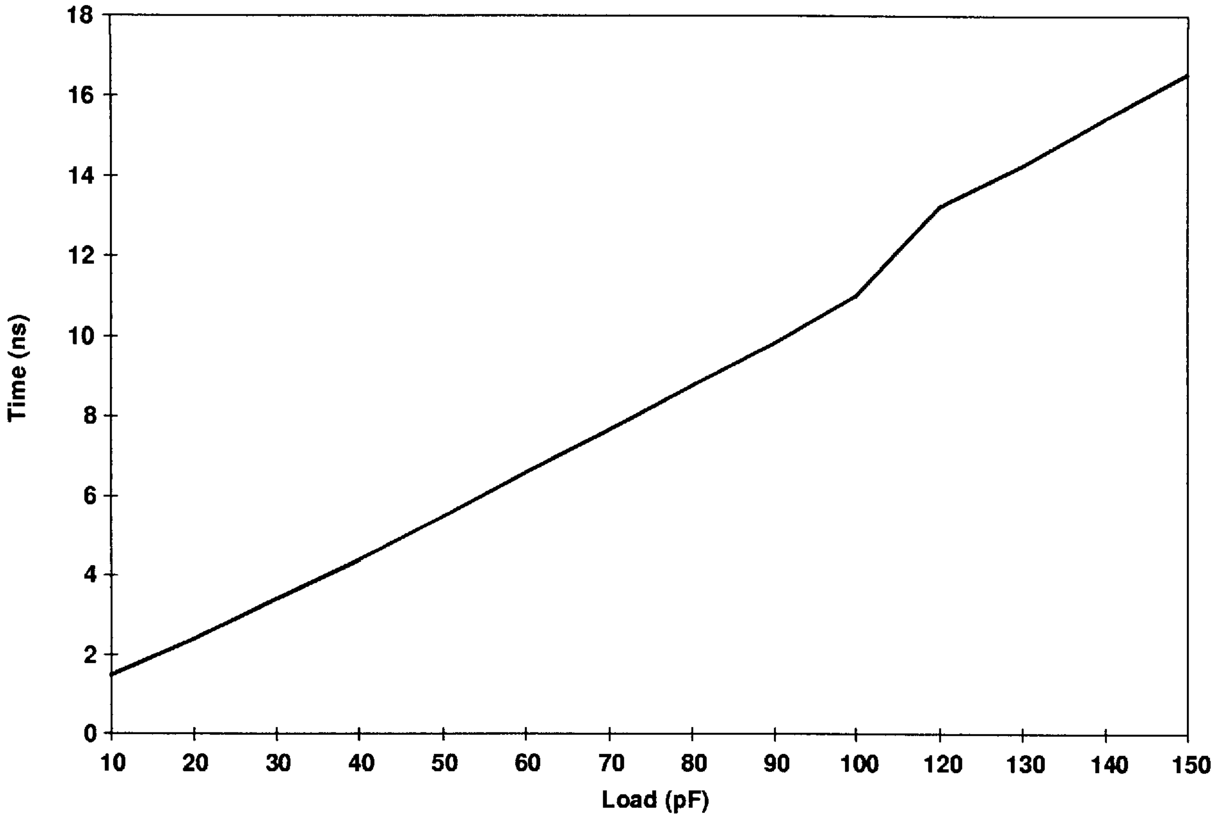


Figure 16. 5-V I/O Drive Type D Fall Time

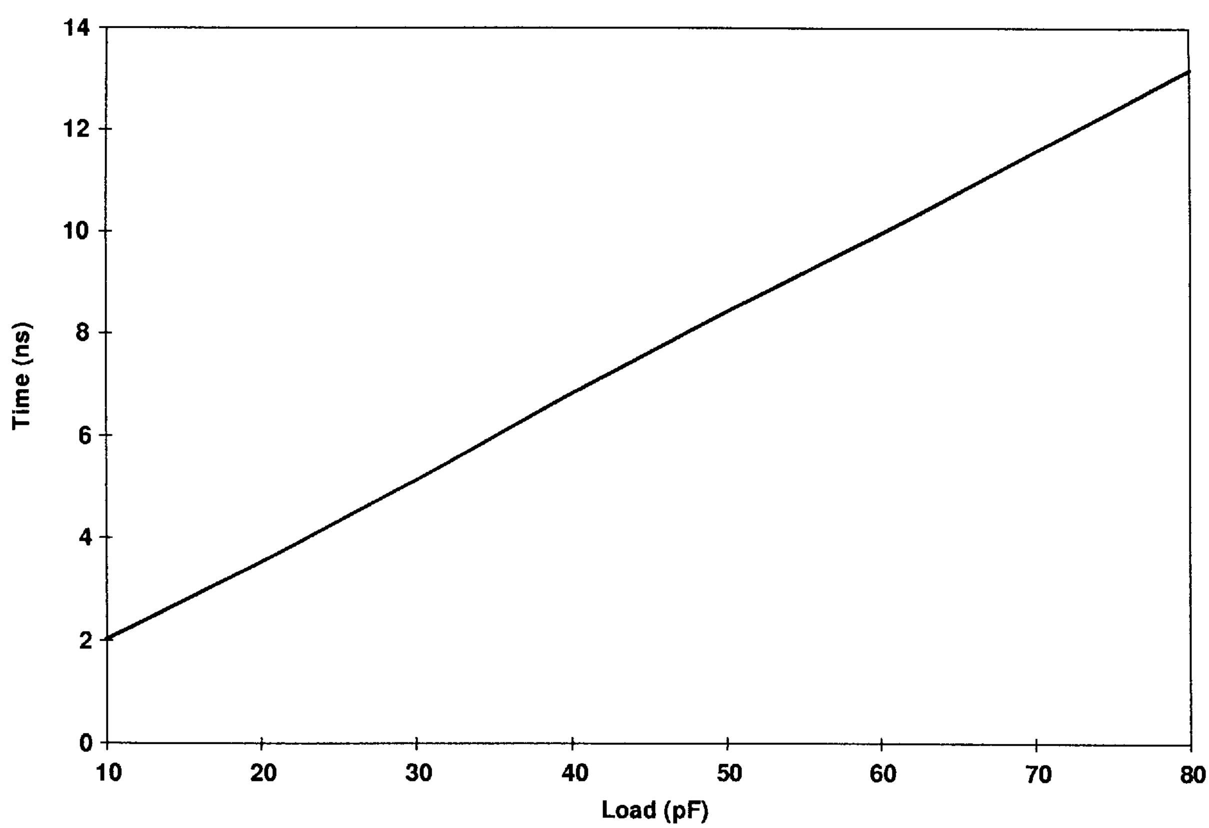


Figure 17. 3.3-V I/O Drive Type C Rise Time

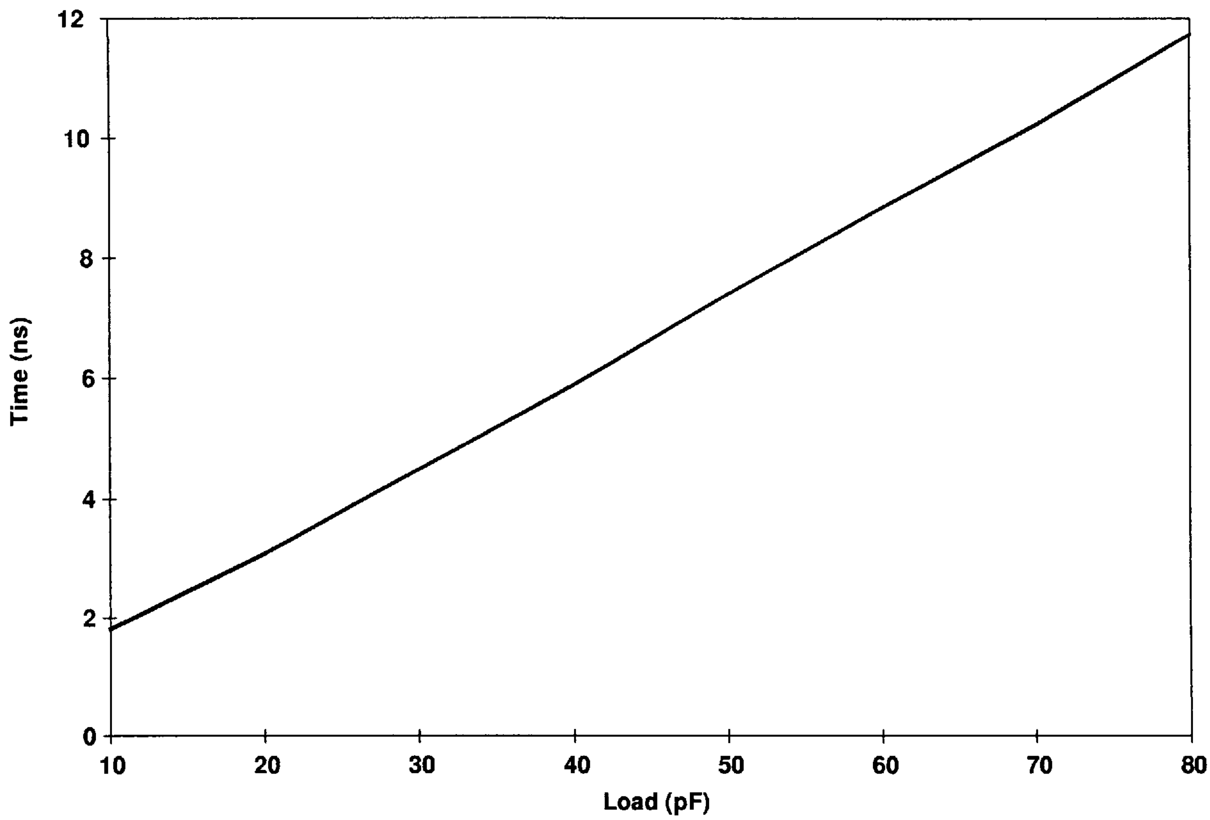


Figure 18. 3.3-V I/O Drive Type C Fall Time

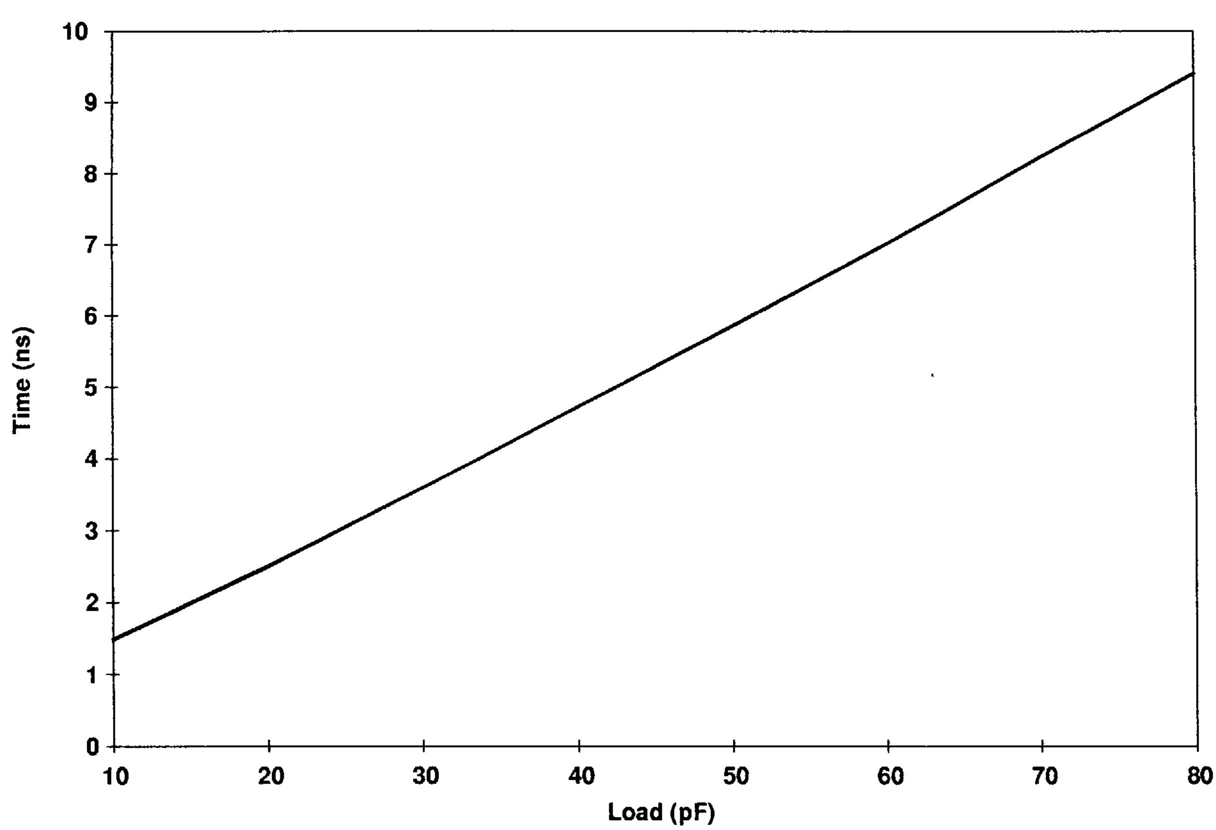


Figure 19. 5-V I/O Drive Type C Rise Time

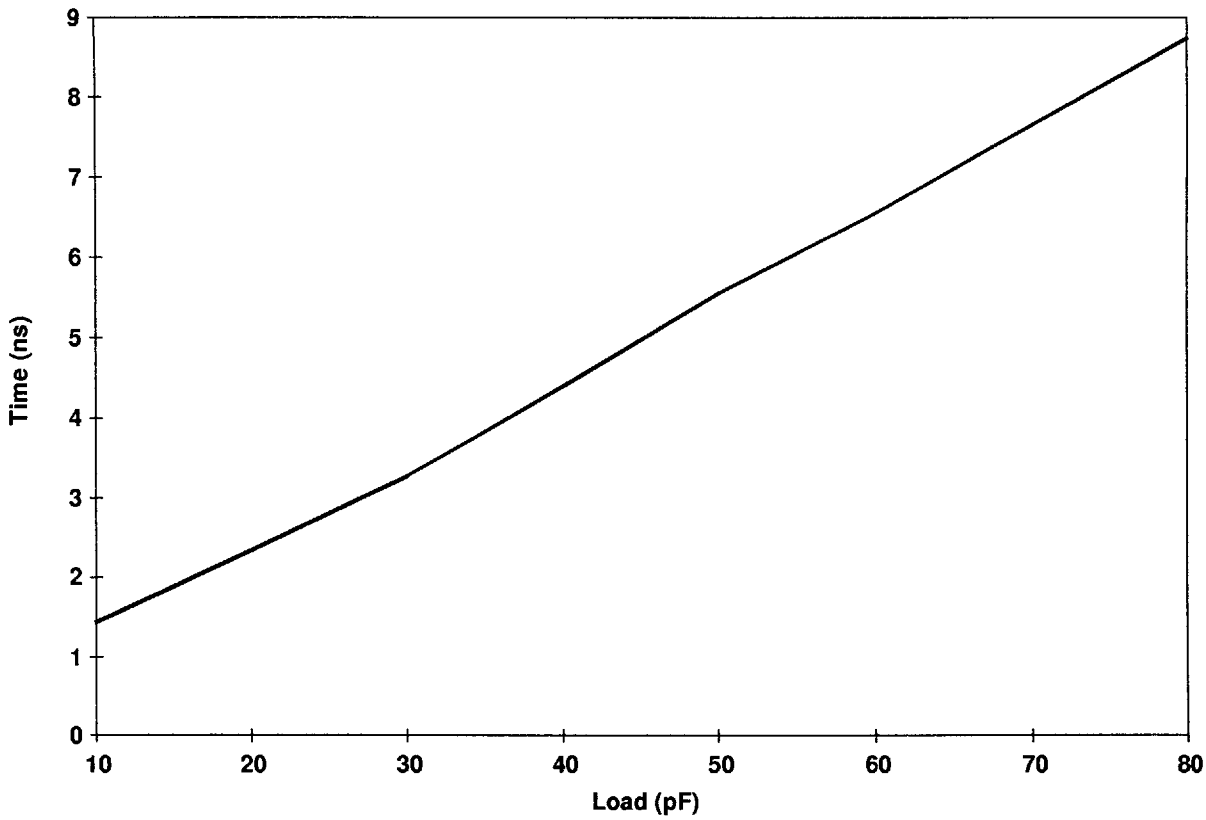


Figure 20. 5-V I/O Drive Type C Fall Time

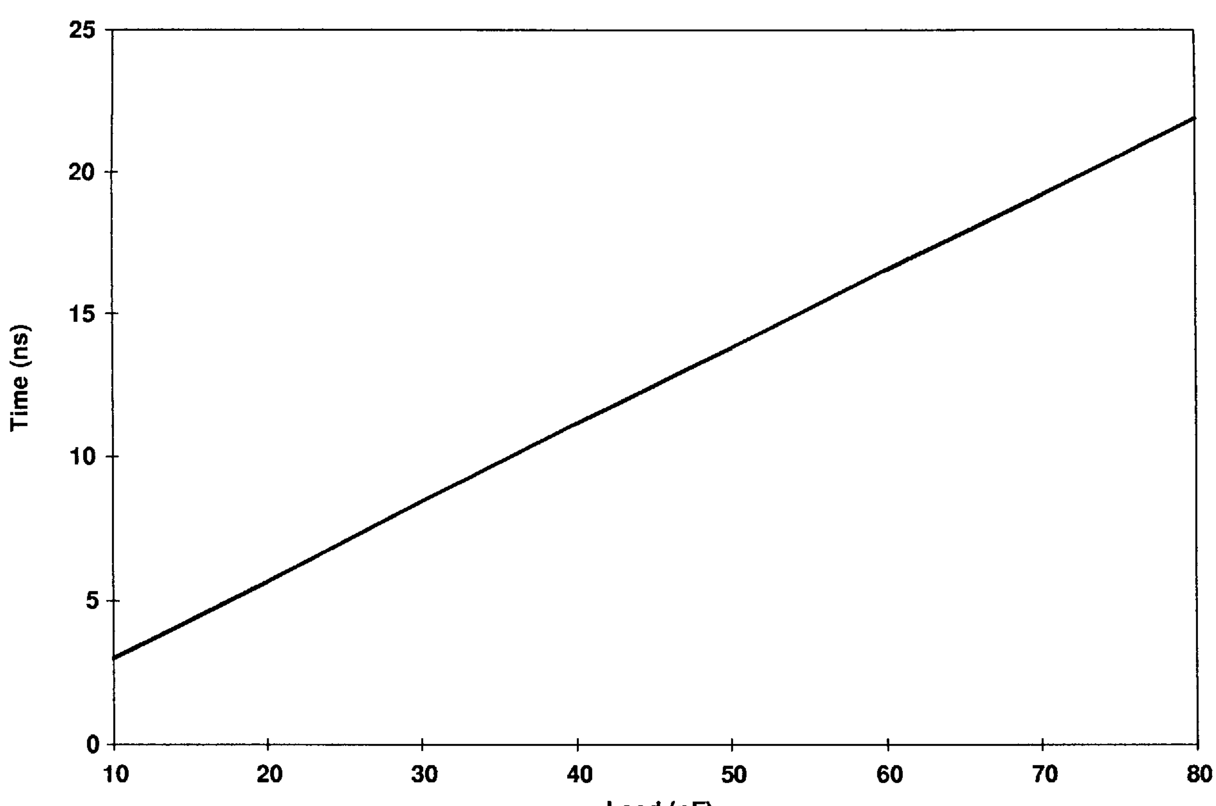


Figure 21. 3.3-V I/O Drive B Rise Time

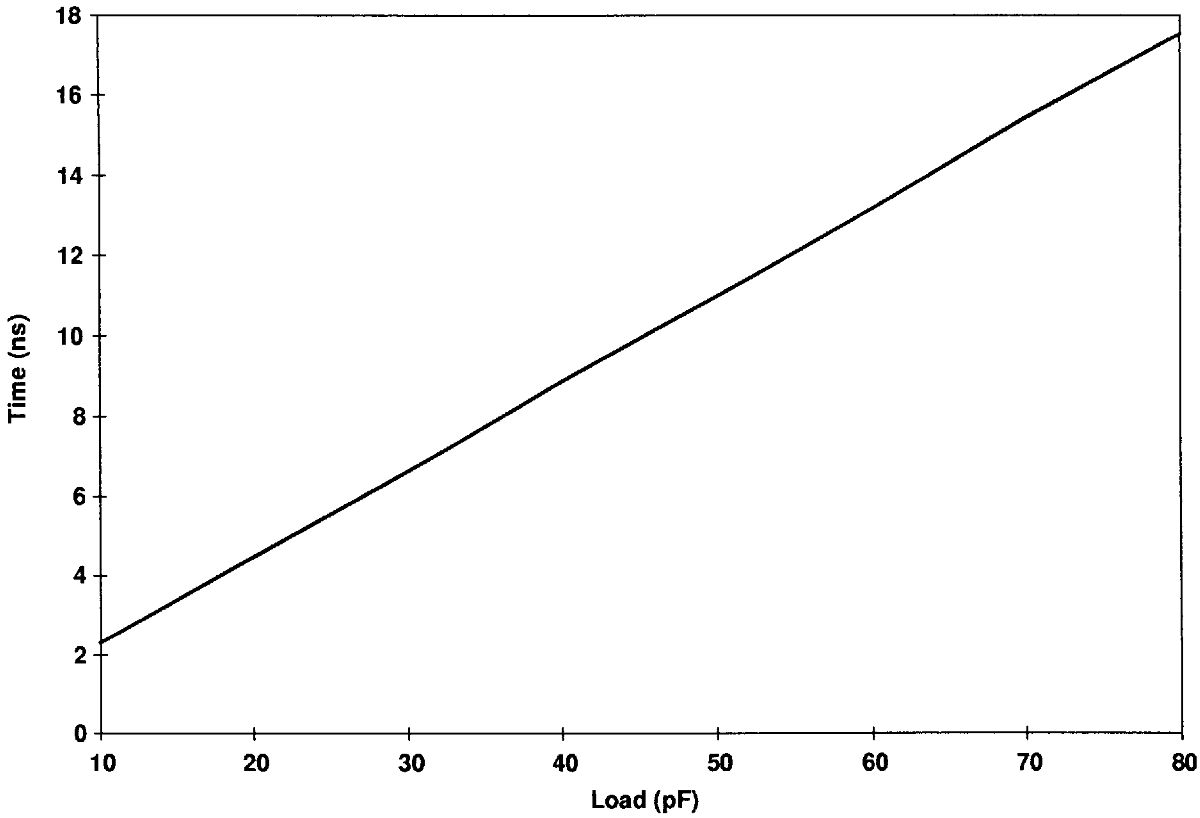


Figure 22. 3.3-V I/O Drive Type B Fall Time

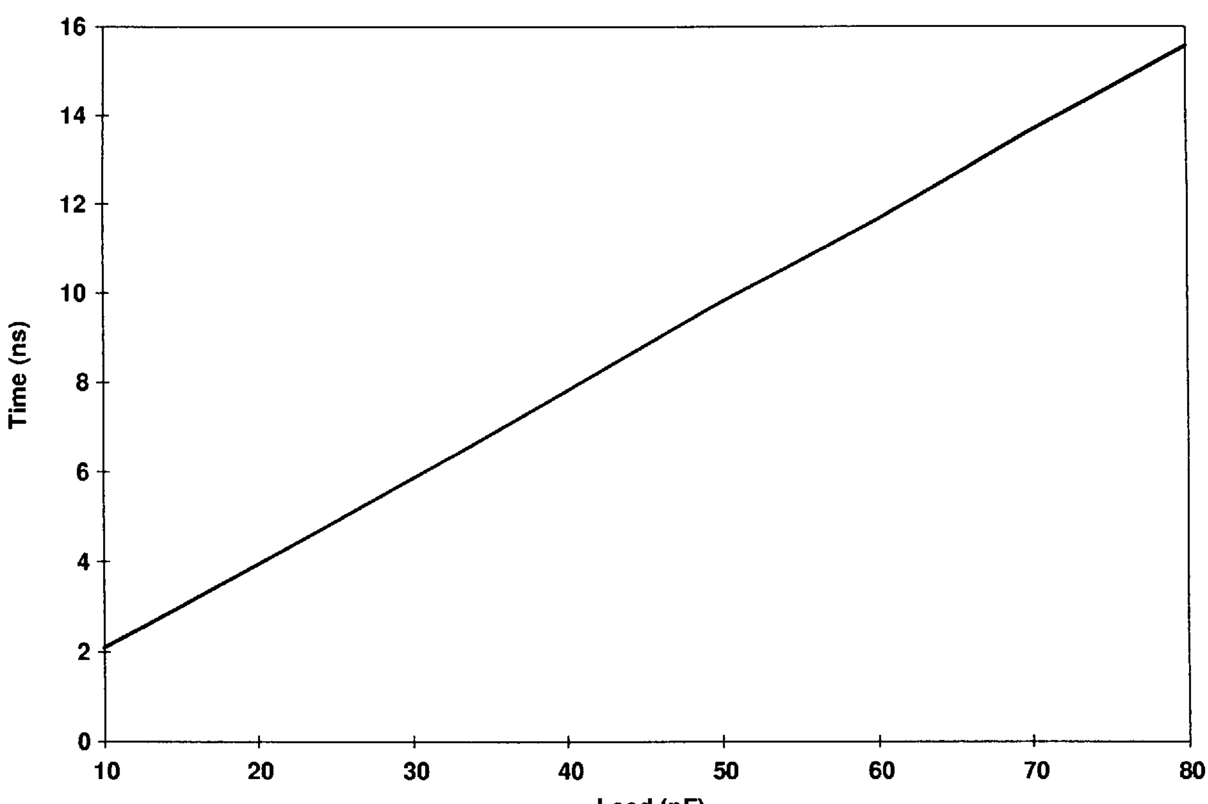


Figure 23. 5-V I/O Drive Type B Rise Time

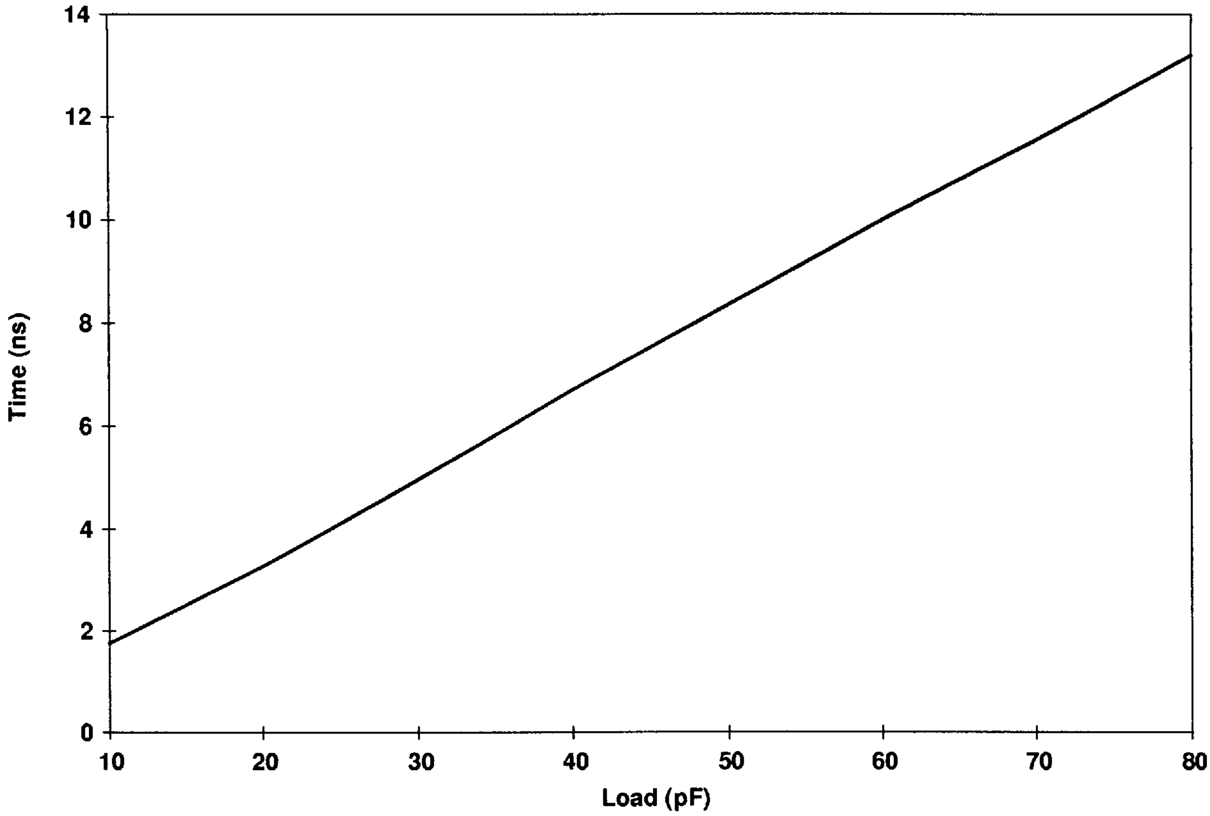


Figure 24. 5-V I/O Drive Type B Fall Time

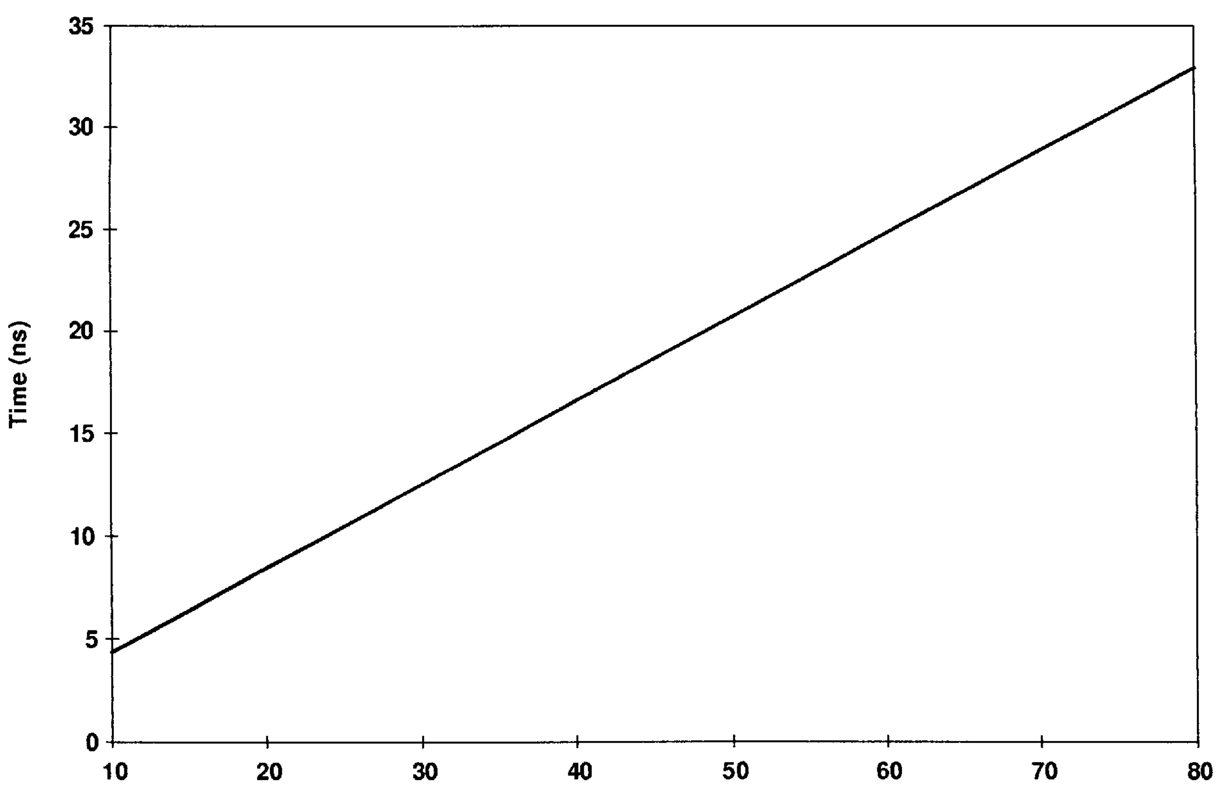


Figure 25. 3.3-V I/O Drive Type A Rise Time

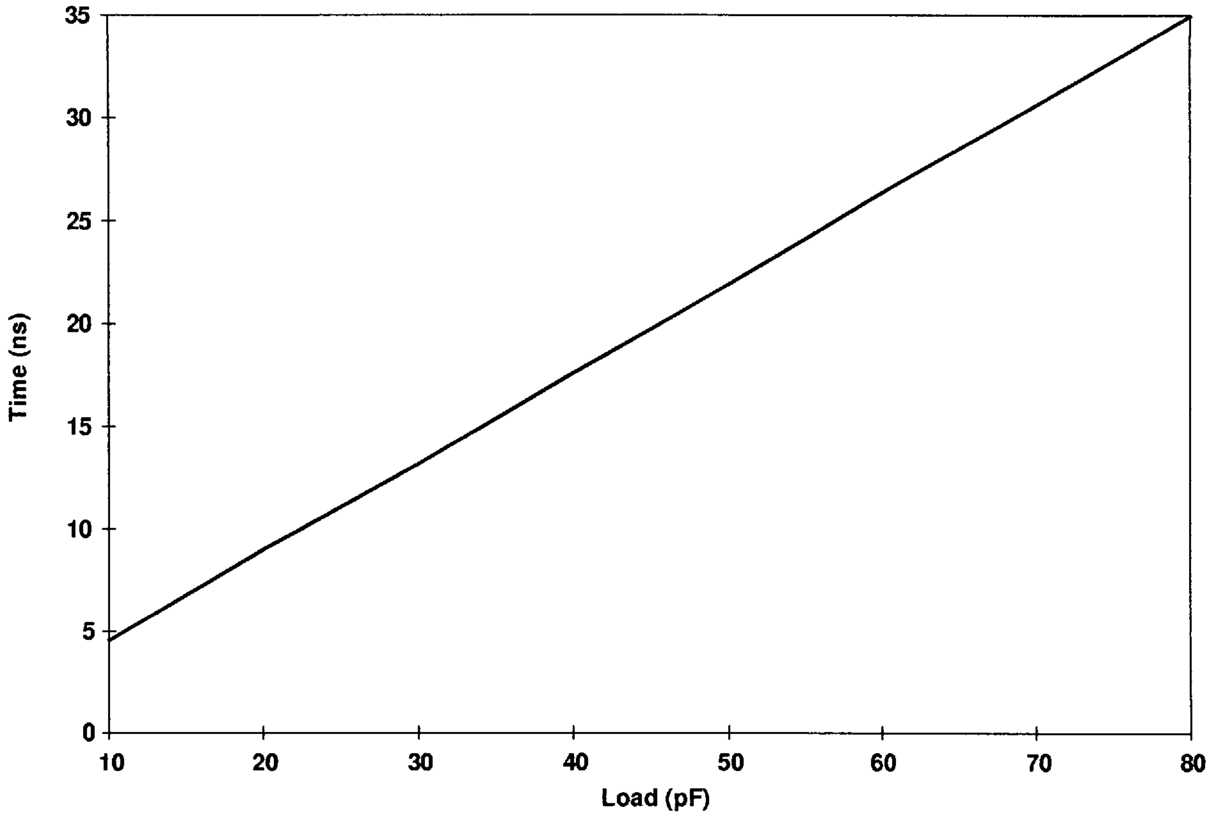


Figure 26. 3.3-V I/O Drive Type A Fall Time

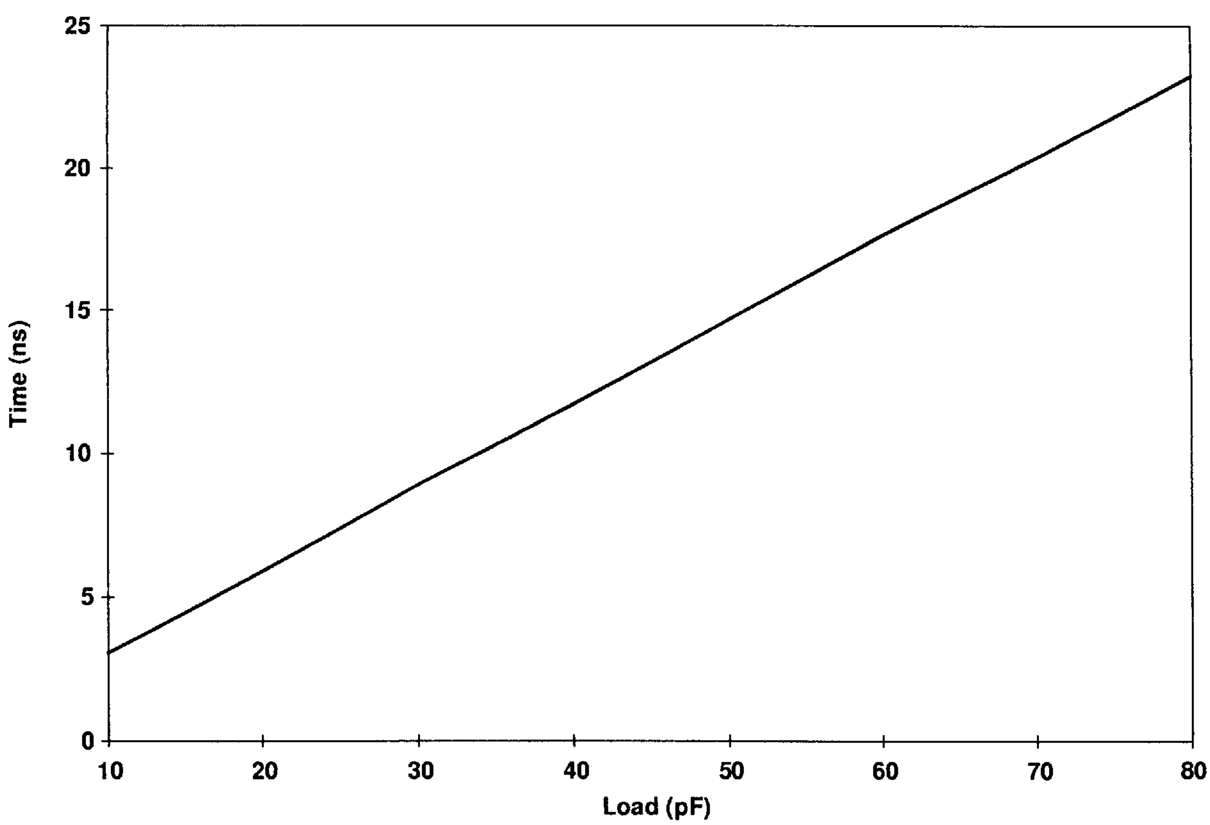


Figure 27. 5-V I/O Drive Type A Rise Time

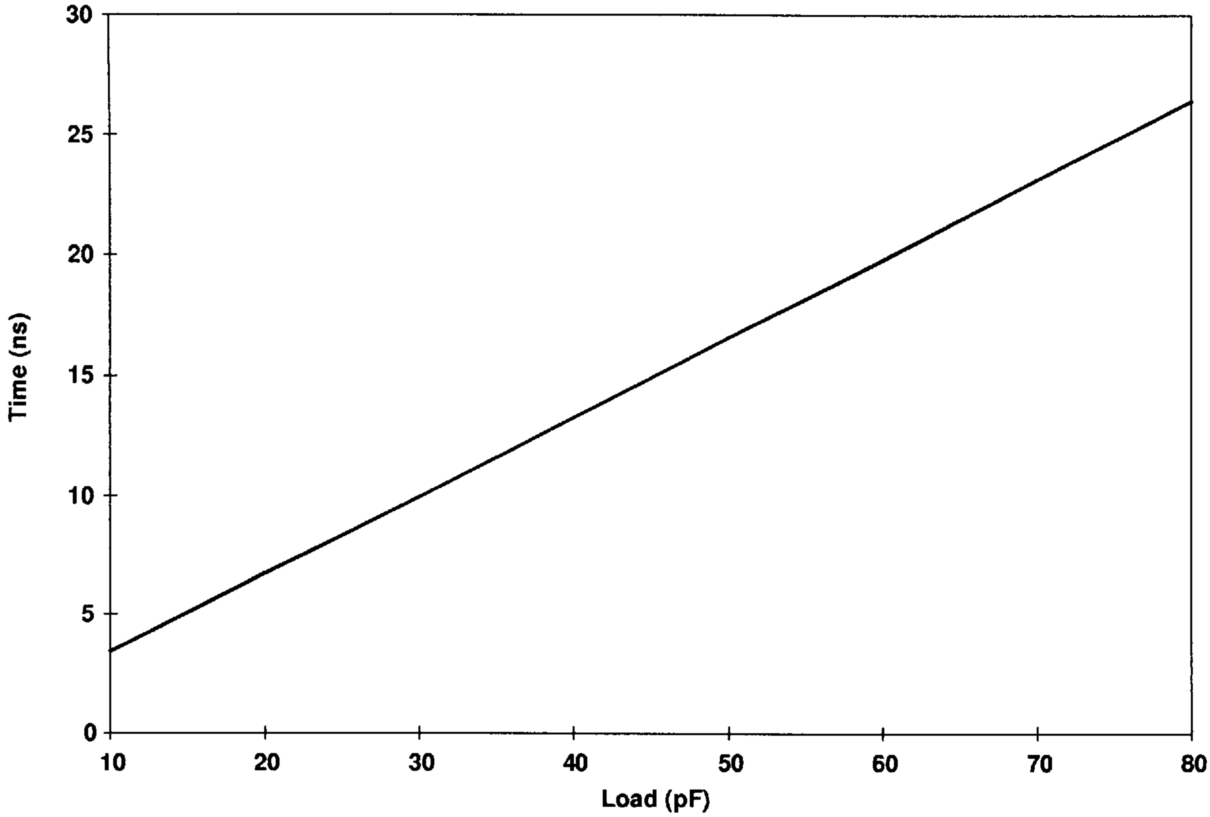


Figure 28. 5-V I/O Drive Type A Fall Time

VOLTAGE PARTITIONING

The Am386SC300 microprocessor supports both 3.3-V system designs and mixed 3.3-V and 5-V system designs. For 3.3-V only operation, all supply pins (VCC, VCC1, VCC5, VMEM, VSYS, VSYS2, and AVCC) should be connected to the 3.3-V DC supply. To operate an interface at 5 V, the VCCIO pins associated with that I/O interface should be connected to 5 V. All supply pins of the same name should be connected to the same voltage plane. The different supply pins and their functions are described in this section.

Refer to the Pin Characteristics section beginning on page 12 of this data sheet for the internal VCC rail (VCCIO) to which each pin is electrically attached.

VCC — These supply pins are used to provide power to the Am386SC300 microprocessor core only. These pins should always be connected to a 3.3-V source.

VCC1 — This supply pin provides power to a subset of the LCD/alternate, power management, and ISA interface pins. This pin can be connected to either a 3.3-V or 5-V source depending on the logic threshold requirements of the external peripherals attached to these interfaces. When connected to the 5-V supply, all outputs with VCC1 as their VCCIO will be 5-V outputs. If connected to 3.3 V, all of these outputs will be 3.3-V outputs.

VCC5 — These supply pins are used to provide a 5-V source for the 5-V input and output pins. If the system design requires that the Am386SC300 microprocessor support 5-V tolerant inputs, then this pin should be connected to a 5-V DC source. This supply pin is the VCCIO for the Parallel Port, Serial Port, and PCMCIA interfaces.

VMEM — This supply pin controls the operating voltage of the memory interface. When connected to the 5-V supply, all outputs to the main memory will be 5-V outputs. This includes the Am386SC300 microprocessor data bus. Therefore, translation buffers may be required when interfacing to 5-V devices on the data bus when the Memory interface is operating at 3.3 V.

VSYS — These supply pins provide power to a subset of the ISA address and command signal pins, external memory chip selects, buffer direction controls, and other miscellaneous functions. These pins can be required to operate at 3.3 V or 5 V depending on the system design.

VSYS2 — This supply pin controls the operating voltage for some of the LCD/alternate function pins. This voltage pin should be connected to either 3.3 V or 5 V depending on the type of bus option selected, the voltage threshold requirements of attached devices, and the state of the other voltage pins associated with the LCD/alternate function interface pins (i.e., VCC1 and VSYS).

AVCC — These supply pins provide power to the analog section of the Am386SC300 microprocessor. They should always be connected to the 3.3-V supply.

CRYSTAL SPECIFICATIONS

The Am386SC300 microprocessor on-chip oscillator is the primary clock source driving all of the on-chip PLL clock generators and the real time clock (RTC) function directly. Externally, a parallel resonant AT cut crystal (32.768 kHz), two capacitors, and two resistors are required for the oscillator to function properly. It is critical that the frequency of the oscillator circuit be as close as possible to the nominal 32.768-kHz frequency for RTC accuracy. By selecting the appropriate external circuit components, this oscillator circuit can be made to operate at very close to the nominal 32.768 kHz.

Figure 29 shows the complete oscillator circuit including the discrete component model for the crystal. In this figure, the external discrete components that must be supplied by the system designer are R_F, R_B, C_D, C_G, and XTAL. R_F is the external feedback resistor for the on-chip amplifier. R_B provides some isolation between the parasitic capacitance of the chip and the crystal. The value of this resistor also has a very small effect on the operating frequency of the circuit. C_D and C_G are the external load capacitors. The value of these capacitors, in conjunction with the other capacitive values discussed below, have the most effect on the operating frequency of this circuit.

The discrete components inside the dotted line represent the circuit model for the crystal with C_0 representing the crystal lead shunt capacitance. The dashed line component C_{STRAY} represents the stray capacitance of the printed circuit board. Typically, a crystal manufacturer provides values for all of the equivalent circuit model components for a given crystal (i.e., L_1, C_1, R_1, and C_0). In addition to these parameters, the manufacturer will provide a load capacitance specification usually designated as C_L. The load capacitance specification is the capacitive load at which the manufacturer has tuned the crystal for the specified frequency. It is therefore required that the load capacitance in the above oscillator circuit is duplicated as closely as possible to the manufacturer's load capacitance specification.

The crystal load capacitance in the above circuit consists of the capacitor network C_0, C_{STRAY}, C_D, and C_G. This network reduces to ($C_0 + C_{STRAY}$) in parallel with the series combination of C_D and C_G. Therefore, the desired series combination of C_D and C_G is equal to $C_L - (C_0 + C_{STRAY})$, where C_L is the crystal manufacturer's load capacitance specification.

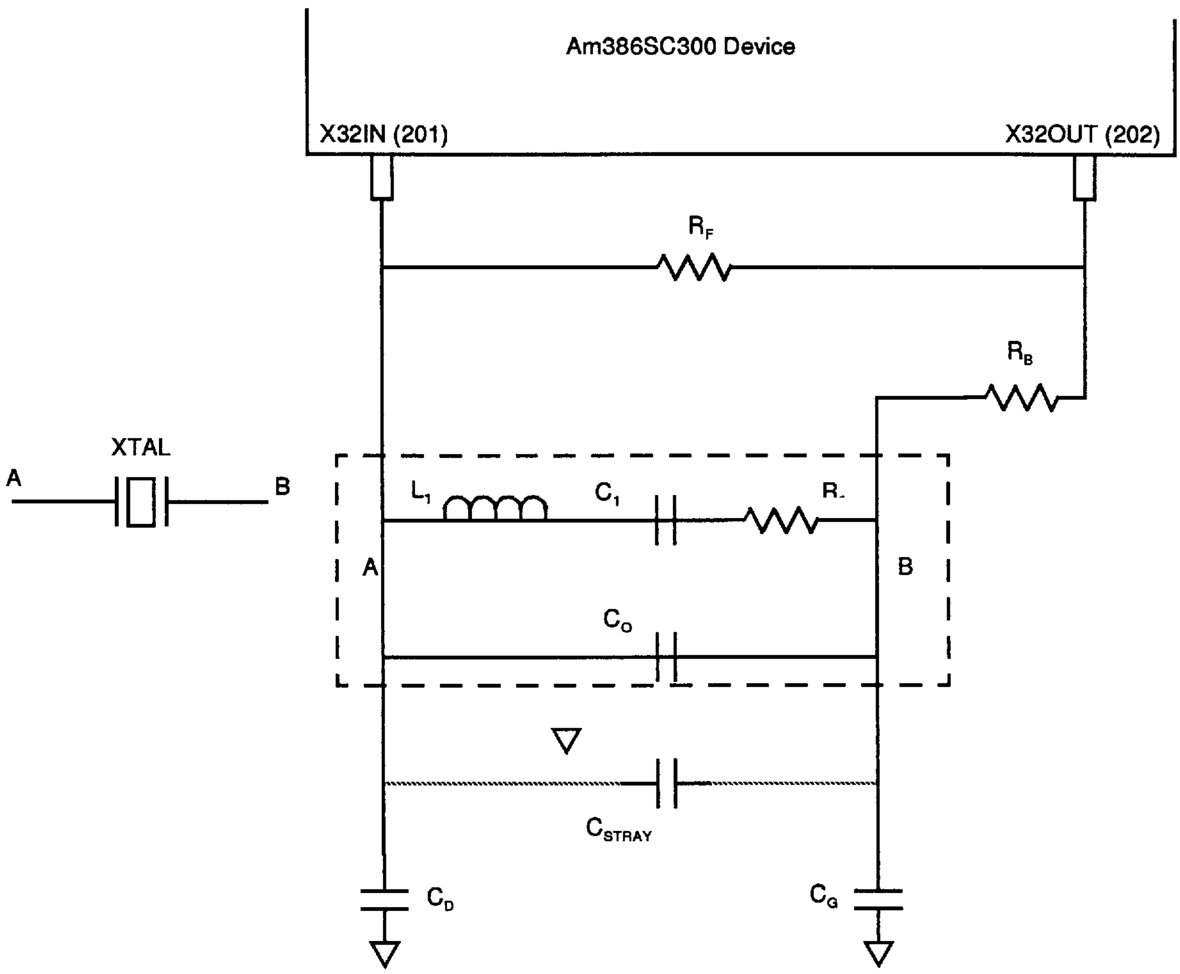


Figure 29. X32 Oscillator Circuit

The series combination of C_D and C_G =

$$\left(\frac{(C_D \times C_G)}{(C_D + C_G)}\right)$$

C_{STRAY} is typically difficult to determine. Some value can be assumed and experimentation will determine the optimal value for C_D and C_G. In determining the external component values to provide the optimal operating frequency, there are some recommended limits to ensure a reasonable start-up time for the oscillator circuit. These limits are shown in Table 35.

Table 35. Recomended Oscillator Component Value Limits

	Minimum	Maximum
R_F	14 MΩ	18 MΩ
R_B	0 Ω	10 KΩ
C_D	10 pF	30 pF
C_G	10 pF	30 pF

LOOP FILTERS

Each of the Phase Locked Loops (PLLs) in the Am386SC300 microprocessor require an external Loop Filter. Figure 30 describes each of the Loop Filters and the recommended component values. The recommended values for the components are shown in Table 36.

The system designer shall include the pads on the printed circuit board to accommodate the future installation/change of C2 and R1. This is recommended because the PLL performance can be affected by the physical circuit board design. In addition, future revisions of the Am386SC300 microprocessor with a modified PLL design may require the addition of these components to the system board.

The component value(s) of the Loop Filter directly affect the acquisition (start up) time of the PLL circuit. With the values recommended, the approximate acquisition time is 200 ms. Therefore, the system designer should program the Clock Control Register at Index 8FH appropriately. Bits 0, 1, and 2 set the PLL restart delay time. When the PLLs are shut off for any reason (i.e., power management), the PLL will be allowed an amount of time equal to that programmed in this register to start up before the PLL outputs are enabled for the internal device logic. A PLL restart delay time of 256 ms should be set in the Clock Control Register.

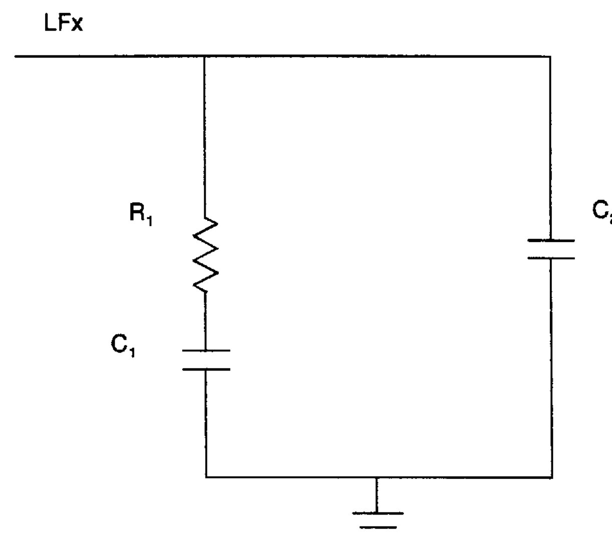
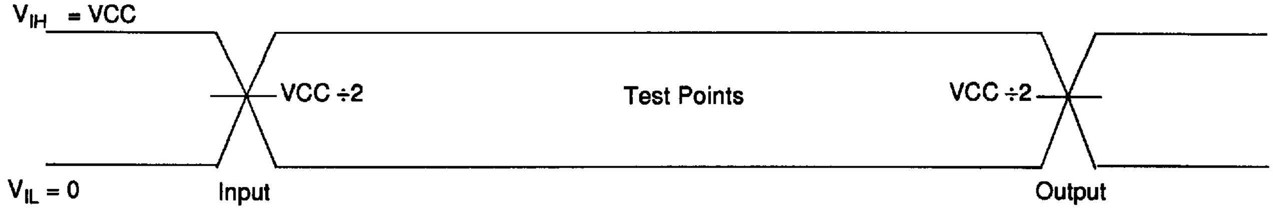


Figure 30. Loop-Filter Component

Table 36. Loop-Filter Component Values

LFx	R_1	C_1	C_2
1	0	0.47 µF	Not Installed
2	0	0.47 µF	Not Installed
3	0	0.47 µF	Not Installed
4	0	0.47 µF	Not Installed

AC SWITCHING TEST WAVEFORMS



AC Testing: Inputs are driven at 3 V for a logic 1 and 0 V for a logic 0.

AC SWITCHING CHARACTERISTICS over COMMERCIAL OPERATING RANGE

Table 37. Power Up Sequencing (See Figures 31, 32, 33, and 34)

Symbol	Parameter Description	Notes	Preliminary			Unit
			Min	Typ	Max	
t1	All VCC valid to $\overline{RESIN}$ and $\overline{IORESET}$ inactive	1		1		s
t2	RSTDRV pulse width		300			µs
t3	$\overline{RESIN}$ and $\overline{IORESET}$ inactive to RSTDRV active		0			ns
t4	VSYS2, VCC1, and VSYS valid delay from VCC5		0			ns
t5	VSYS2, VCC1, VSYS, and optionally VMEM valid to $\overline{IORESET}$ inactive		5			µs
t6	VCC5, VSYS2, VCC1, VSYS hold time from $\overline{IORESET}$ active		5			µs
t7	VCC5 hold time from VSYS2, VCC1, and VSYS inactive				0	ns

Notes:
Voltage sequencing on power-up for the Am386SC300 device should be observed as follows:

a. VCC

b. All VCC Clamp sources (VCC, VMEM, VSYS, VCC5, and AVCC)

c. All VCCIO Sources (VCC5, VMEM, VSYS, VCC1, VSYS2, and AVCC). The reverse is true when powering down. For any particular I/O pin, the VCCIO may come up simultaneously with the VCC Clamp, but should never proceed VCC Clamp. Refer to the Pin Characteristics table (page 10) for detailed I/O information.

1. This parameter is dependent on the 32-KHz oscillator start-up time. The oscillator start-up time is dependent on the external component values used, board layout, and power supply noise.

2. $\overline{RESIN}$ remains inactive during Micro Power Off mode and Micro Power Off mode exit.

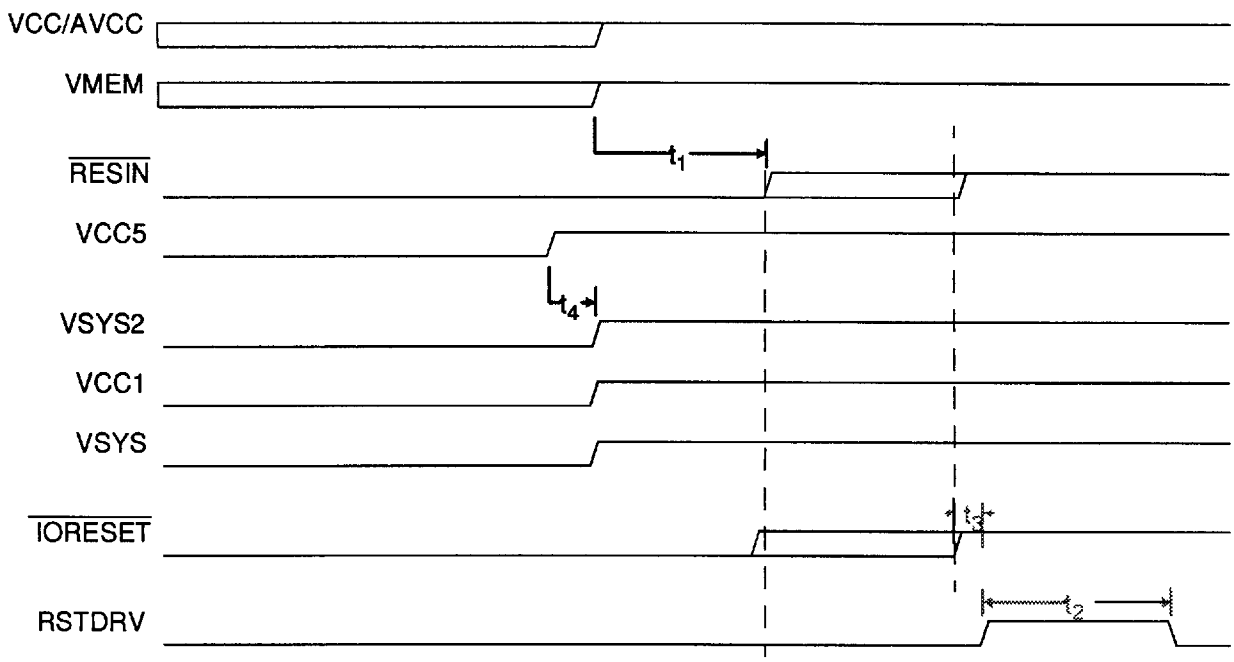


Figure 31. Power-Up Sequence Timing

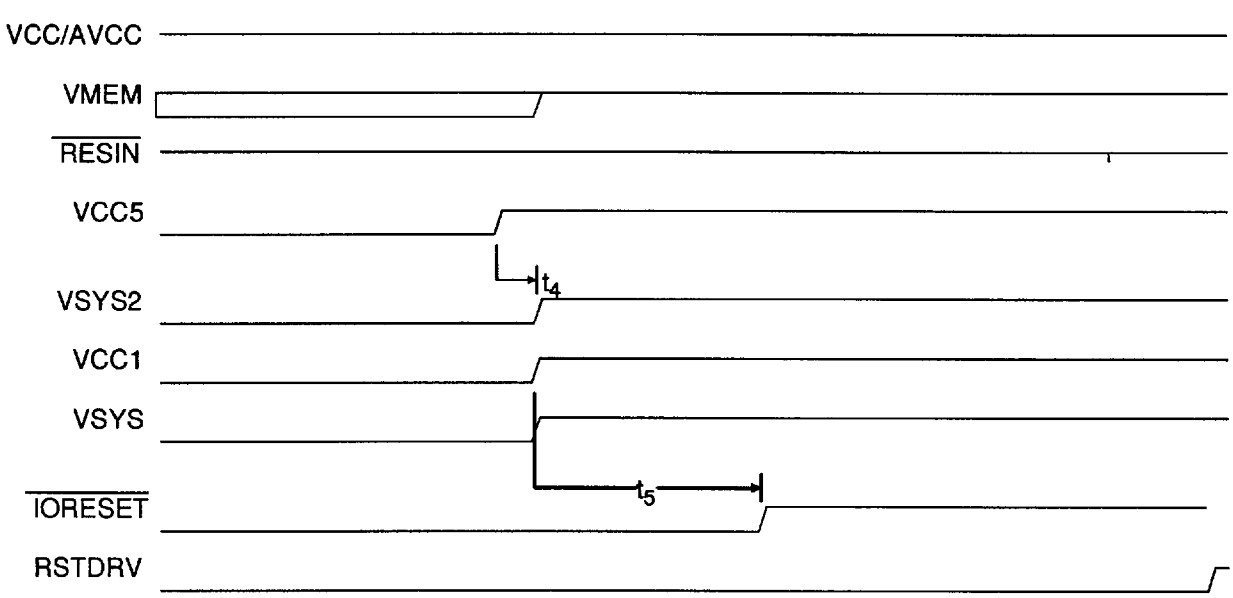
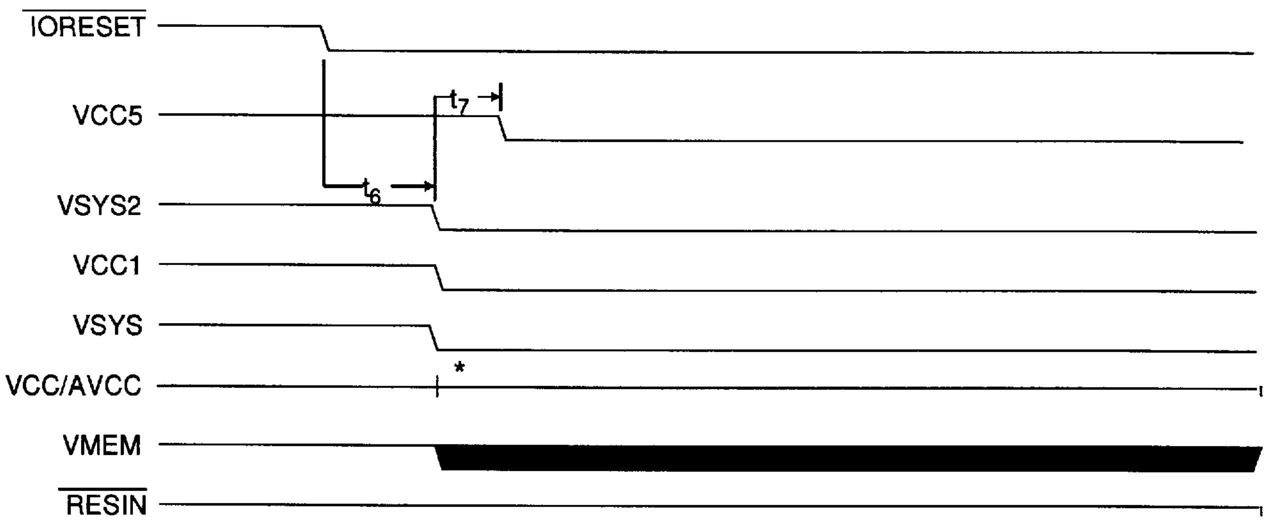
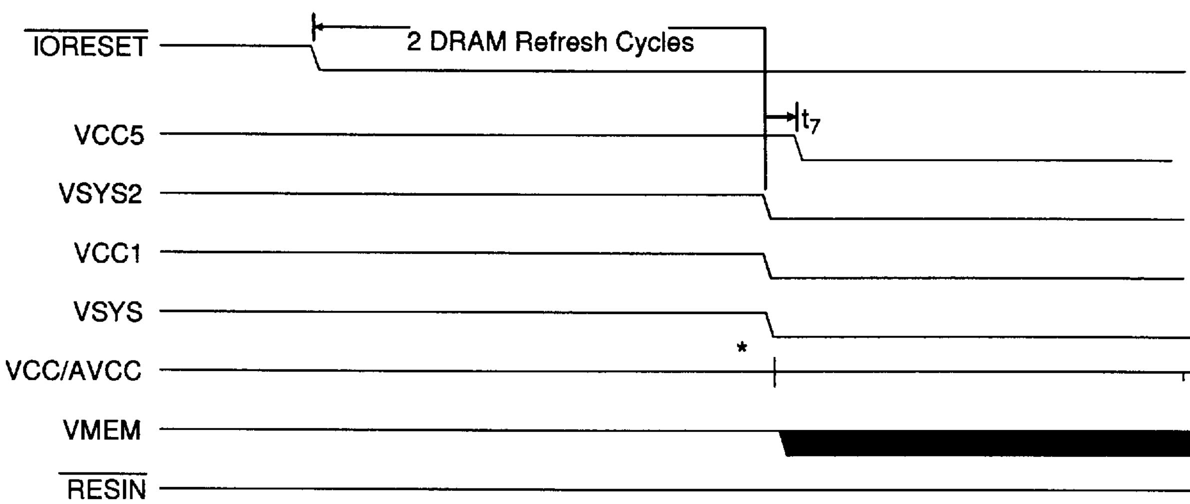


Figure 32. Micro Power Off Mode Exit



Note: * *A secondary power source could be applied at this time*

Figure 33. Entering Micro Power Off Mode (DRAM Refresh Disabled)



Note: * *A secondary power source could be applied at this time*

Figure 34. Entering Micro Power Off Mode (DRAM Refresh Enabled)

Table 38. DRAM Memory Interface

Symbol	Parameter Description	Notes	Preliminary Min	Preliminary Typ	Preliminary Max	Unit
t30	MA valid setup to $\overline{\text{RAS}}$ Low		0			ns
t31	MA hold from $\overline{\text{RAS}}$ Low		10			ns
t32	MA setup to $\overline{\text{CAS}}$ Low		0			ns
t33	$\overline{\text{RAS}}$ hold from $\overline{\text{CAS}}$ Low		20			ns
t34	$\overline{\text{RAS}}$ precharge from $\overline{\text{CAS}}$ High		10			ns
t36	$\overline{\text{RAS}}$ precharge		50			ns
t37	$\overline{\text{CAS}}$ precharge (Page mode)		10			ns
t38	MA hold from $\overline{\text{CAS}}$ active		15			ns
t39	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay		20			ns
t40	$\overline{\text{RAS}}$ pulse width		70		10,000	ns
t41	$\overline{\text{CAS}}$ pulse width		20		10,000	ns
t42	$\overline{\text{WE}}$ setup to $\overline{\text{CAS}}$ Low		0			ns
t43	$\overline{\text{WE}}$ hold from $\overline{\text{CAS}}$ Low		15			ns
t44	$\overline{\text{CAS}}$ hold from $\overline{\text{RAS}}$ Low		70			ns
t45	$\overline{\text{CAS}}$ cycle time (page mode)		45			ns
t46	$\overline{\text{CAS}}$ Low to D15–D0 valid (read)				20	ns
t47	D15–D0 hold from $\overline{\text{CAS}}$ High (read)		0			ns
t48	D15–D0 setup to $\overline{\text{CAS}}$ Low (write)		0			ns
t49	D15–D0 hold from $\overline{\text{CAS}}$ Low (write)		15			ns
t50	$\overline{\text{CAS}}$ Low to $\overline{\text{RAS}}$ Low (refresh)		10			ns
t51	$\overline{\text{CAS}}$ hold from $\overline{\text{RAS}}$ Low (refresh)		70			ns
t53	$\overline{\text{RAS}}$ pulse width (suspend refresh)		80			ns

Note:
These timings are based on 33-MHz operation and 70-ns DRAM.

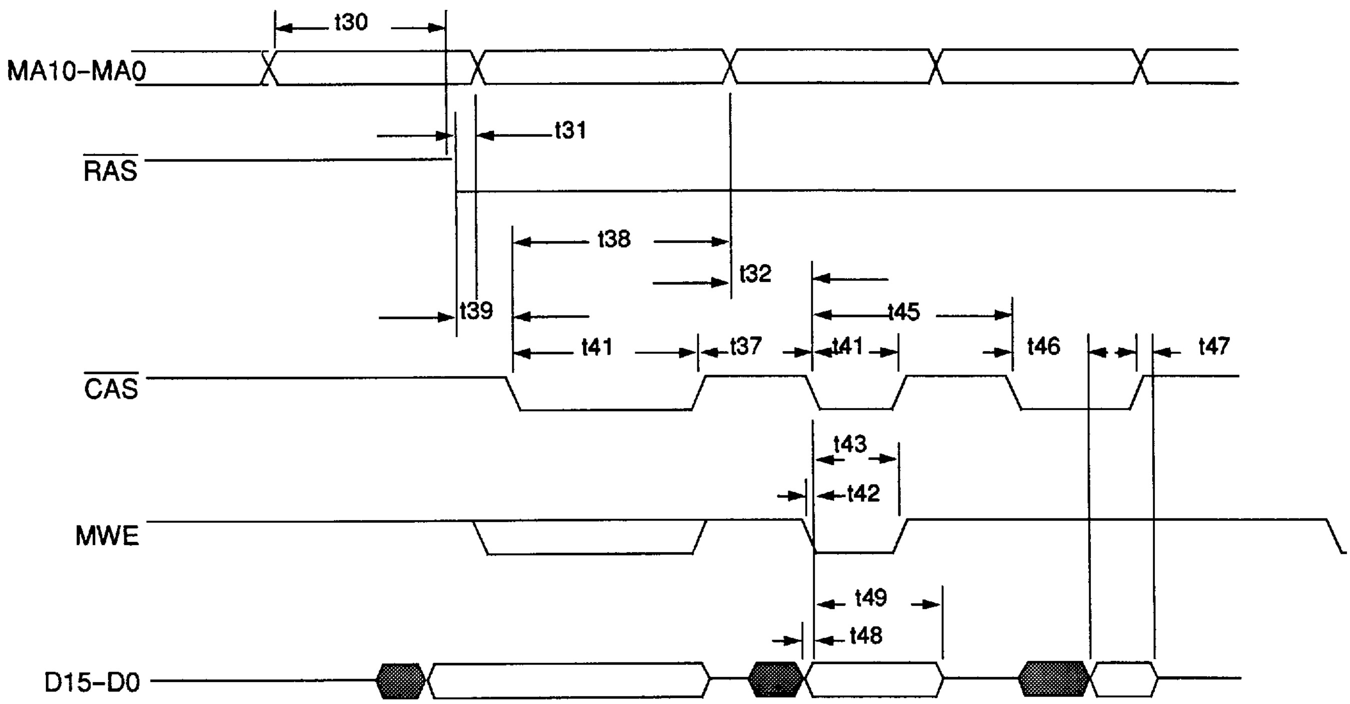


Figure 35. DRAM Timings, Page Hit

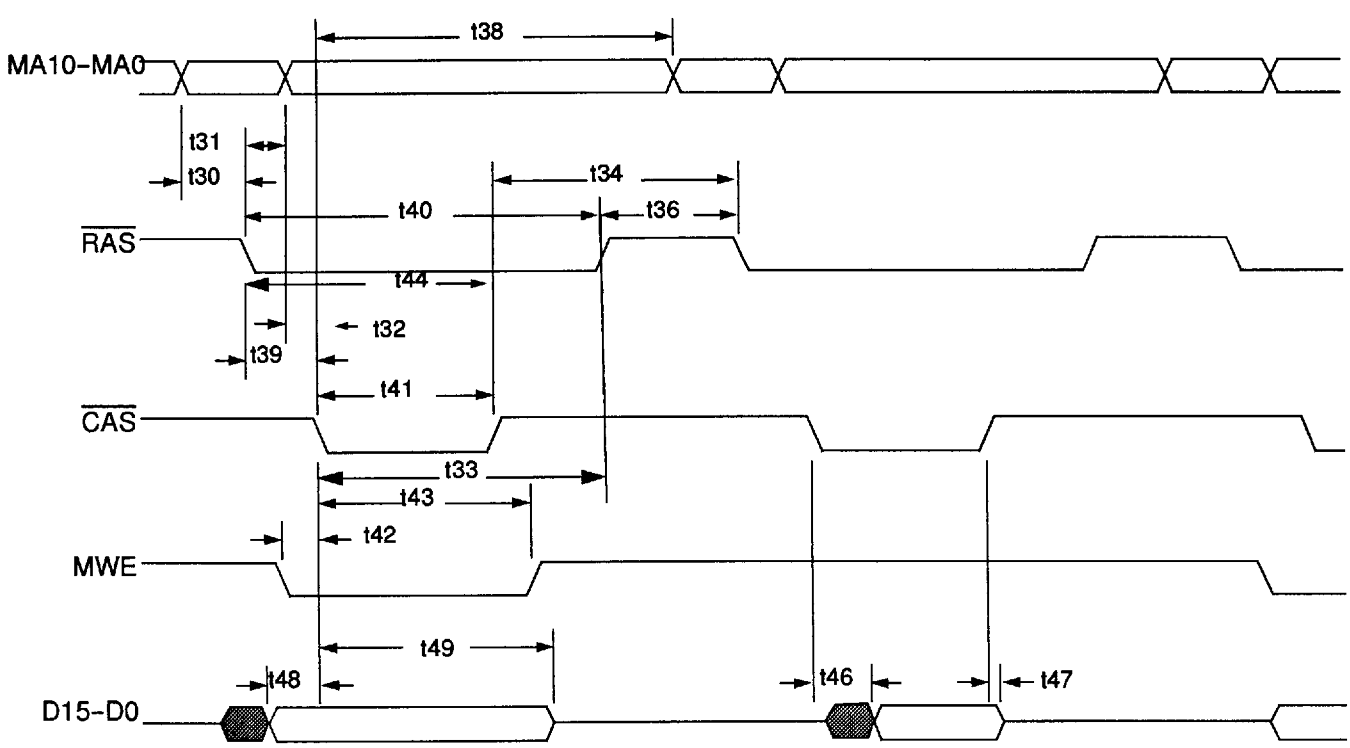


Figure 36. DRAM Timings, Page Miss

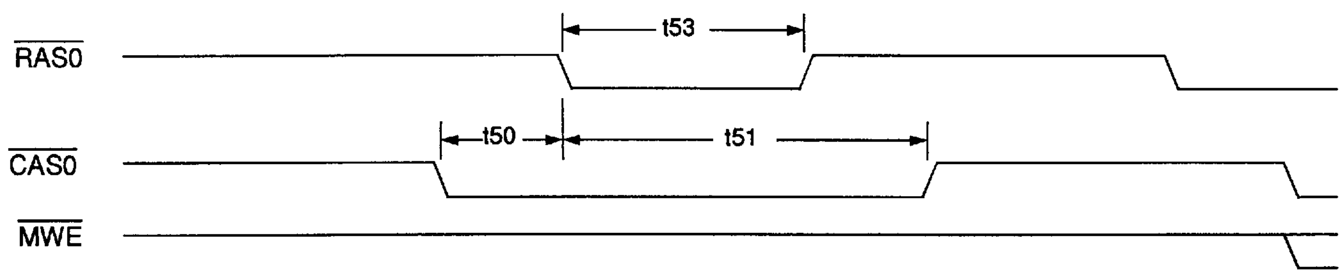


Figure 37. DRAM Timings, Refresh Cycle

Table 39. Local Bus Interface (See Figure 38)

Symbol	Parameter Description	Notes	Preliminary			Unit
			Min	Typ	Max	
t1	CPUCLK period		14			ns
t2	CPUCLK pulse width low		7			ns
t3	CPUCLK pulse width high		7			ns
t4	ADS delay from CPUCLK		3		15	ns
t5	A[23–1] BLE, BHE, W/R,D/C, M/IO delay from CPUCLK		5		23	ns
t6a	LDEV valid from A or control (non-zero wait-state)		2		20	ns
t6b	LDEV valid from A or control (zero wait-state)		2		18	ns
t7	LRDY valid from CPUCLK		2		12	ns
t8	LRDY high-impedence from CPUCLK		0		5	ns
t9	CPURDY delay from CPUCLK		5		26	ns
t10	CPURDY high-impedence from CPUCLK		0		5	ns
t11	D15 - D0 setup to CPUCLK (read)		7			ns
t12	D15 - D0 hold from CPUCLK (read)		0		0	ns
t13	D15 - D0 valid from CPUCLK (write)		5		20	ns

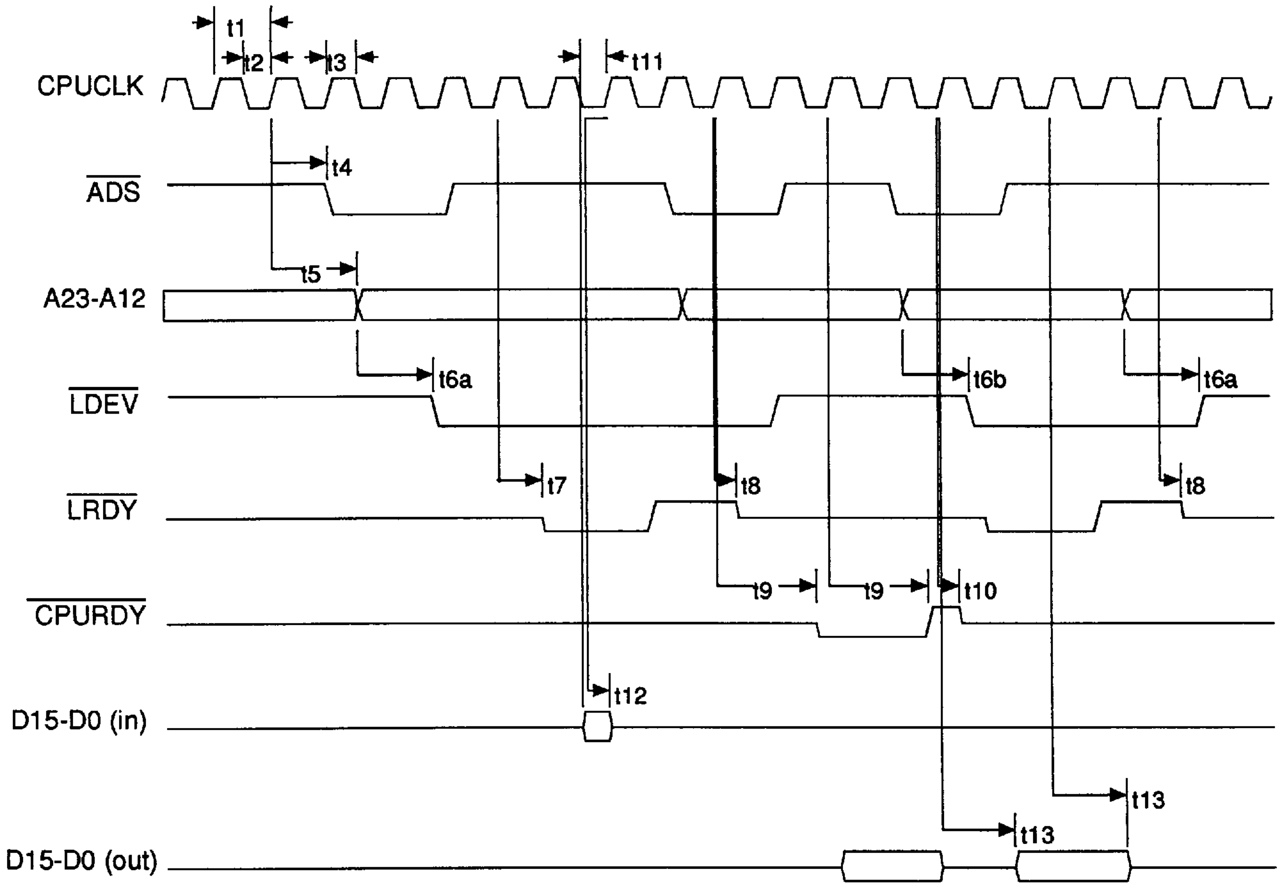


Figure 38. Local Bus Interface

Table 40. Video RAM/LCD Interface

Symbol	Parameter Description	Notes	Preliminary			Unit
			Min	Typ	Max	
t81	DSMD hold from DSMA change		5			ns
t82	Display RAM read cycle pulse width		85			ns
t83	DSMD active from $\overline{\text{DSWE}}$ active				50	ns
t84	DSMD setup to $\overline{\text{DSWE}}$ inactive		0			ns
t85	DSMA hold from $\overline{\text{DSWE}}$ inactive		5			ns
t86	DSMD hold from $\overline{\text{DSWE}}$ inactive		0			ns
t87	Display RAM write cycle pulse width		65			ns
t88	DSMD tri-state delay from $\overline{\text{DSOE}}$ high		5		30	ns
t89	DSMD delay from $\overline{\text{DSOE}}$ active		5		30	ns
t90	Panel data setup to CP2 (data clock)		5			ns
t91	Panel data hold from CP2 (data clock)		10			ns
t92	Panel data delay from CP2 (data clock)				10	ns
t93	CP2 allowance time from CP1 (latch pulse)		65			ns
t94	CP1 allowance time from CP2		65			ns
t95	FRM setup time		520			ns
t96	FRM hold time		520			ns
t97	DSMA setup to $\overline{\text{DSWE}}$ active		0			ns

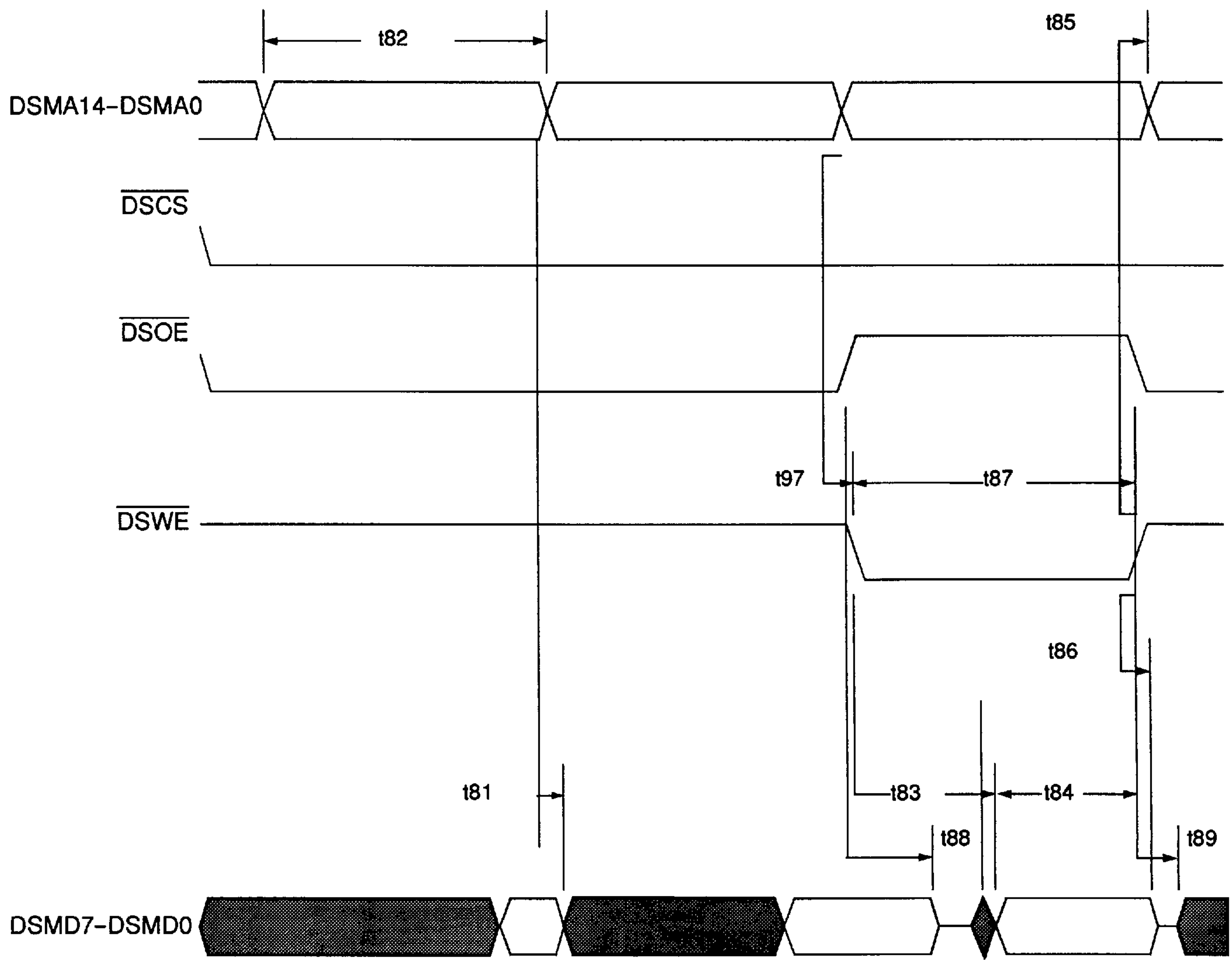


Figure 39. Display SRAM Timings

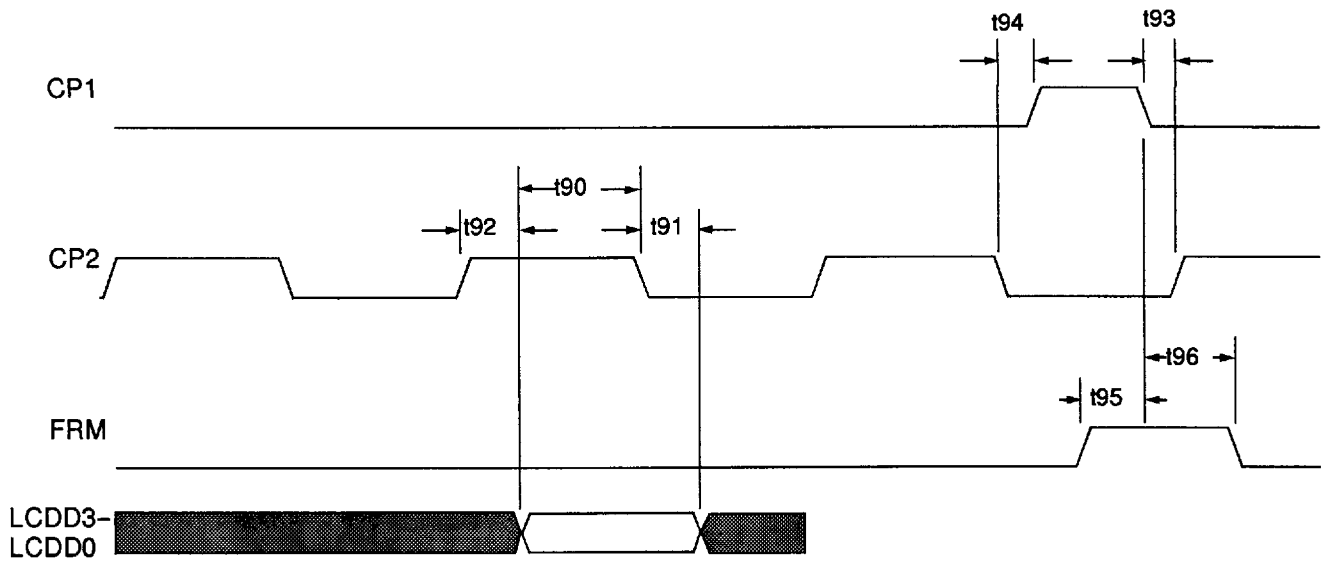


Figure 40. LCD Interface Timings

Table 41. PCMCIA Memory Read Cycle

Symbol	Parameter Description	Notes	Preliminary			Unit
			Min	Typ	Max	
t1a	Data setup before $\overline{\text{MEMR}}$ inactive (8-bit)		40			ns
t1b	Data setup before $\overline{\text{MEMR}}$ inactive (16-bit)		25			ns
t2	Data hold following $\overline{\text{MEMR}}$		0			ns
t3	$\overline{\text{MEMR}}$ width time		550			ns
t4a	Address setup before $\overline{\text{MEMR}}$ (8-bit)	1	155			ns
t4b	Address setup before $\overline{\text{MEMR}}$ (16-bit)		60			ns
t5	Address hold following $\overline{\text{MEMR}}$	2, 3	0			ns
t6a	$\overline{\text{MCE}}$ setup before $\overline{\text{MEMR}}$ (8-bit)	4	175			ns
t6b	$\overline{\text{MCE}}$ setup before $\overline{\text{MEMR}}$ (16-bit)	4	45			ns
t7	$\overline{\text{MCE}}$ hold after $\overline{\text{MEMR}}$	2, 4	0			ns
t8	$\overline{\text{MEMR}}$ inactive from $\overline{\text{WAIT\_AB}}$ inactive		120			ns
t9	$\overline{\text{WAIT\_AB}}$ delay falling from $\overline{\text{MEMR}}$				35	ns
t10	$\overline{\text{WAIT\_AB}}$ pulse width time	5			12,000	ns
t11	ICDIR setup before $\overline{\text{MEMR}}$		–1			ns
t12	ICDIR hold after $\overline{\text{MEMR}}$		0			ns
t13	$\overline{\text{DBUFOE}}$ setup before $\overline{\text{MEMR}}$		–2			ns
t14	$\overline{\text{DBUFOE}}$ hold after $\overline{\text{MEMR}}$		–2			ns
t15a	ENDIRH, ENDIRL setup before $\overline{\text{MEMR}}$ (8-bit)		170			ns
t15b	ENDIRH, ENDIRL setup before $\overline{\text{MEMR}}$ (16-bit)		45			ns
t16	ENDIRH, ENDIRL hold from $\overline{\text{MEMR}}$		–4			ns

Notes:
These timings are based on default device settings and required initial programming. These timings may be modified via the device wait state control and command delay register. (See the Élan Am386SC300 Programmer's Reference Manual.*)*

1. *Violates for 600-ns (3.3 V) PCMCIA read cycle only.*
2. *PCMCIA Spec is 35 ns for 600-ns cycle, 20 ns for 250, 200, and 15 ns for a 100-ns cycle.*
3. *If PCMCIA is buffered, this hold time may be increased by propagation delay through the buffer.*
4. *If the PCMCIA address buffer is controlled via the MCE signals, the output disable/enable delay of the buffer will affect the address setup and hold from $\overline{\text{MEMR}}$.*
5. *$\overline{\text{WAIT\_AB}}$ asserted for greater that 10 µs may cause a DRAM $\overline{\text{RAS}}$ low (max) to be violated if the "extended" PCMCIA cycle occurs during a DRAM page hit. (See the t_{RASC} max parameter for a particular DRAM.) The $\overline{\text{RAS}}$ active timer (10 µs) will not force $\overline{\text{RAS}}$ inactive while the "extended" PCMCIA cycle is occurring.*

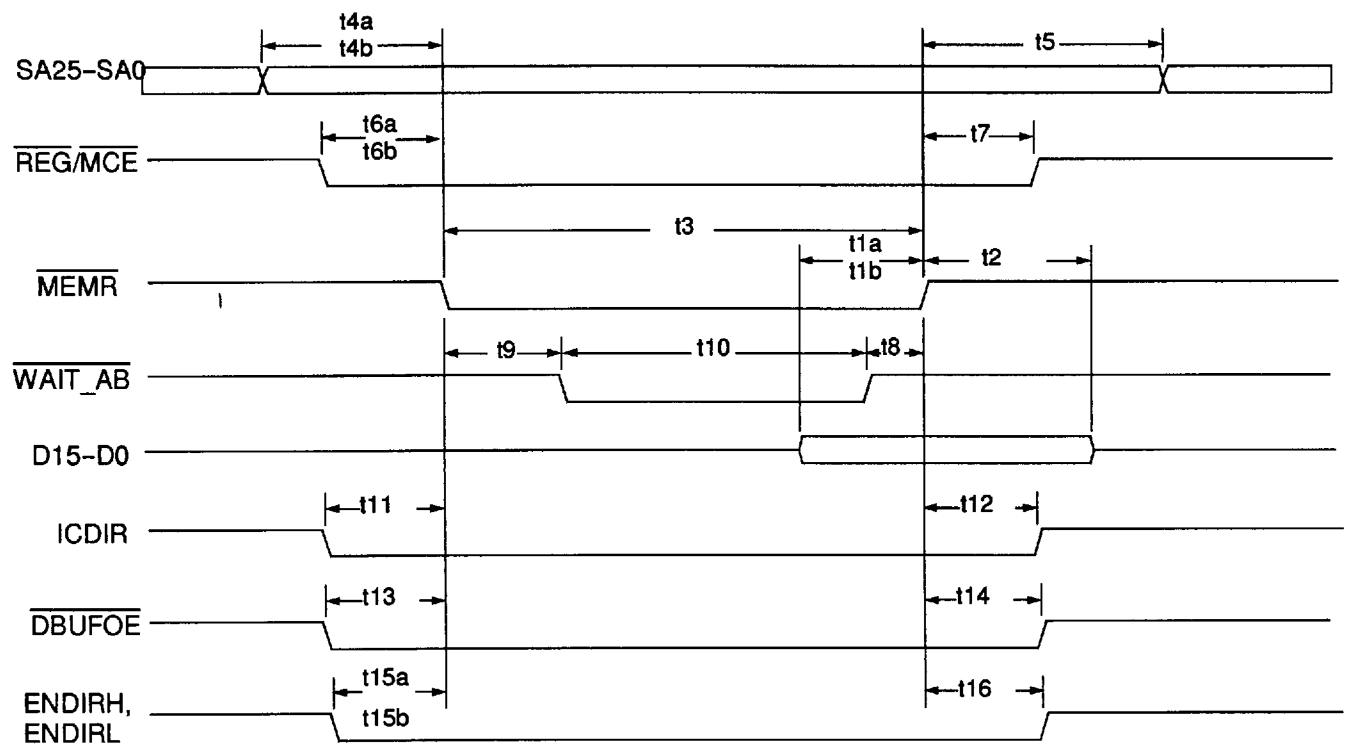


Figure 41. PCMCIA Memory Read Cycle

Table 42. PCMCIA Memory Write Cycle

Symbol	Parameter Description	Notes	Preliminary Min	Preliminary Typ	Preliminary Max	Units
t2	Data hold following $\overline{\text{MEMW}}$		50			ns
t3	$\overline{\text{MEMW}}$ width time		500			ns
t4a	Address setup before $\overline{\text{MEMW}}$ (8-bit)		150			ns
t4b	Address setup before $\overline{\text{MEMW}}$ (16-bit)		60			ns
t5	Address hold following $\overline{\text{MEMW}}$		50			ns
t6a	$\overline{\text{MCE}}$ setup before $\overline{\text{MEMW}}$ (8-bit)		175			ns
t6b	$\overline{\text{MCE}}$ setup before $\overline{\text{MEMW}}$ (16-bit)		45			ns
t7	$\overline{\text{MCE}}$ hold after $\overline{\text{MEMW}}$		40			ns
t8a	Output Enable ($\overline{\text{MEMR}}$) setup before $\overline{\text{MEMW}}$ (8-bit)		200			ns
t8b	Output Enable ($\overline{\text{MEMR}}$) setup before $\overline{\text{MEMW}}$ (16-bit)		100			ns
t9a	Output Enable ($\overline{\text{MEMR}}$) hold after $\overline{\text{MEMW}}$ (8-bit)		250			ns
t9b	Output Enable ($\overline{\text{MEMR}}$) hold after $\overline{\text{MEMW}}$ (16-bit)		150			ns
t10	$\overline{\text{MEMW}}$ inactive from $\overline{\text{WAIT\_AB}}$ inactive		100			ns
t11	$\overline{\text{WAIT\_AB}}$ delay falling from $\overline{\text{MEMW}}$				35	ns
t12	$\overline{\text{WAIT\_AB}}$ pulse width time	1			12,000	ns
t13a	$\overline{\text{DBUFOE}}$ setup before $\overline{\text{MEMW}}$ (8-bit)		150			ns
t13b	$\overline{\text{DBUFOE}}$ setup before $\overline{\text{MEMW}}$ (16-bit)		50			ns
t14	$\overline{\text{DBUFOE}}$ hold after $\overline{\text{MEMW}}$		50			ns

Notes:
These timings are based on default device settings and required initial programming. These timings may be modified via the device wait state control and command delay registers. (See the Élan Am386SC300 Programmer's Reference Manual).

1. *$\overline{\text{WAIT\_AB}}$ asserted for greater that 10 µs may cause a DRAM $\overline{\text{RAS}}$ Low (max) to be violated if this "extended" PCMCIA cycle occurs during a DRAM page hit. (See the t_{RASC} max parameter for a particular DRAM.) The $\overline{\text{RAS}}$ active timer (10 µs) will not force $\overline{\text{RAS}}$ inactive while the "extended" PCMCIA cycle is occurring.*

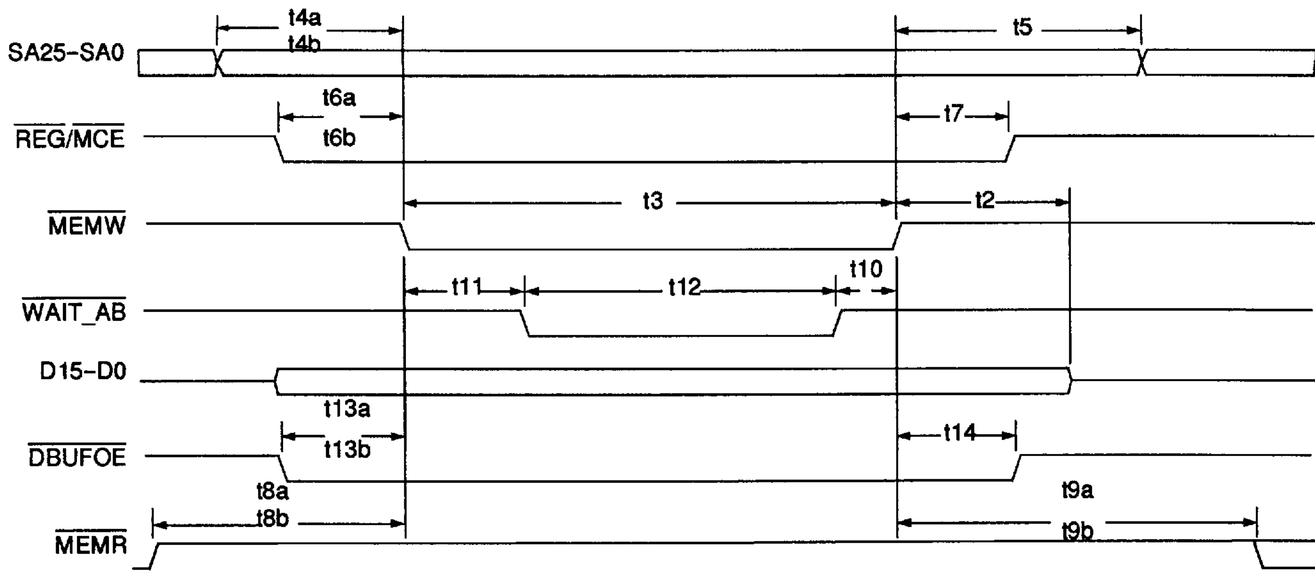


Figure 42. PCMCIA Memory Write Cycle

Table 43. PCMCIA I/O Read Cycle

Symbol	Parameter Description	Notes	Preliminary			Units
			Min	Typ	Max	
t1	Data setup before $\overline{\text{IOR}}$		40			ns
t2	Data hold following $\overline{\text{IOR}}$		0			ns
t3a	$\overline{\text{IOR}}$ width time (8-bit)		560			ns
t3b	$\overline{\text{IOR}}$ width time (16-bit)		280			ns
t4a	Address setup before $\overline{\text{IOR}}$ (8-bit)		150			ns
t4b	Address setup before $\overline{\text{IOR}}$ (16-bit)		115			ns
t5	Address hold following $\overline{\text{IOR}}$	1, 2	–1			ns
t6a	$\overline{\text{MCEL}}$ setup before $\overline{\text{IOR}}$ (8-bit)	3	160			ns
t6b	$\overline{\text{MCEL}}$ setup before $\overline{\text{IOR}}$ (16-bit)		100			ns
t7	$\overline{\text{MCE}}$ hold after $\overline{\text{IOR}}$	2, 3	5			ns
t8	$\overline{\text{REG}}$ setup before $\overline{\text{IOR}}$		5			ns
t9	$\overline{\text{REG}}$ hold after $\overline{\text{IOR}}$		0			ns
t10	$\overline{\text{IOIS16}}$ delay falling from Address				35	ns
t11	$\overline{\text{IOIS16}}$ delay rising from Address				35	ns
t12	$\overline{\text{WAIT\_AB}}$ delay falling from $\overline{\text{IOR}}$				35	ns
t13	$\overline{\text{WAIT\_AB}}$ pulse width time	4			12,000	ns
t14	ICDIR setup before $\overline{\text{IOR}}$		–5			ns
t15	ICDIR hold after $\overline{\text{IOR}}$		0			ns
t16	$\overline{\text{DBUFOE}}$ setup before $\overline{\text{IOR}}$		–3			ns
t17	$\overline{\text{DBUFOE}}$ hold after $\overline{\text{IOR}}$		–3			ns
t18a	ENDIRH, ENDIRL setup before $\overline{\text{IOR}}$ (8-bit)		170			ns
t18b	ENDIRH, ENDIRL setup before $\overline{\text{IOR}}$ (16-bit)		110			ns
t19	ENDIRH, ENDIRL hold from $\overline{\text{IOR}}$		–6			ns
t20	$\overline{\text{MCEH}}$ delay from $\overline{\text{IOCS16}}$ active				50	ns
t21	$\overline{\text{IOR}}$ inactive from $\overline{\text{WAIT\_AB}}$ inactive		100			ns

0257525 0048651 510

Notes:
These timings are based on default device settings and required initial programming. These timings may be modified via the device wait state control and command delay register. (See the Élan Am386SC300 Programmer's Reference Manual.*)*

1. *If PCMCIA is buffered, this hold time may be increased by propagation delay through the buffer.*
2. *PCMCIA Spec. is 20 ns (min) for 5-V I/O cards.*
3. *If the PCMCIA address buffer is controlled via the MCE signals, the output disable/enable delay of the buffer will affect the address setup and hold from MEMR.*
4. *WAIT_AB asserted for greater that 10 µs may cause a DRAM RAS low (max) to be violated if the "extended" PCMCIA cycle occurs during a DRAM page hit. (See the t_{RASC} max parameter for a particular DRAM.) The RAS active timer (10 µs) will not force RAS inactive while the "extended" PCMCIA cycle is occurring.*

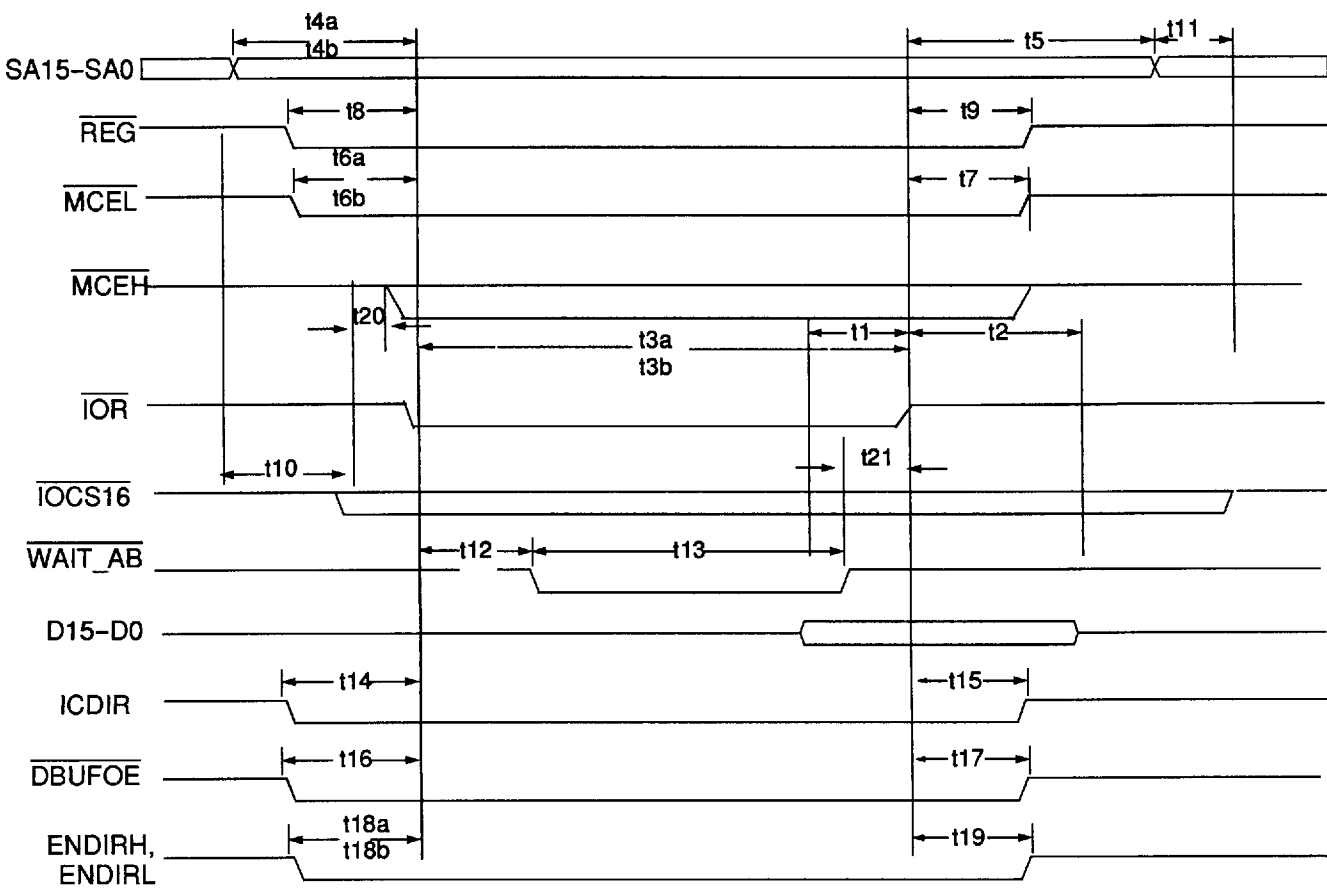


Figure 43. PCMCIA I/O Read Cycle

Table 44. PCMCIA I/O Write Cycle

Symbol	Parameter Description	Notes	Preliminary Min	Preliminary Typ	Preliminary Max	Units
t1	Data setup before $\overline{\text{IOW}}$ active		25			ns
t2	Data hold following $\overline{\text{IOW}}$		50			ns
t3a	$\overline{\text{IOW}}$ width time (8-bit)		440			ns
t3b	$\overline{\text{IOW}}$ width time (16-bit)		165			ns
t4a	Address setup before $\overline{\text{IOW}}$ (8-bit)		175			ns
t4b	Address setup before $\overline{\text{IOW}}$ (16-bit)		165			ns
t5	Address hold following $\overline{\text{IOW}}$		50			ns
t6a	$\overline{\text{MCEL}}$ setup before $\overline{\text{IOW}}$ (8-bit)		215			ns
t6b	$\overline{\text{MCEL}}$ setup before $\overline{\text{IOW}}$ (16-bit)		160			ns
t7	$\overline{\text{MCE}}$ hold after $\overline{\text{IOW}}$		50			ns
t8a	$\overline{\text{REG}}$ setup before $\overline{\text{IOW}}$ (8-bit)		230			ns
t8b	$\overline{\text{REG}}$ setup before $\overline{\text{IOW}}$ (16-bit)		170			ns
t9	$\overline{\text{REG}}$ hold after $\overline{\text{IOW}}$		50			ns
t10	$\overline{\text{IOCS16}}$ delay falling from Address				35	ns
t11	$\overline{\text{IOCS16}}$ delay rising from Address				35	ns
t12	$\overline{\text{WAIT\_AB}}$ delay falling from $\overline{\text{IOW}}$				35	ns
t13	$\overline{\text{WAIT\_AB}}$ pulse width time	1			12,000	ns
t14a	$\overline{\text{DBUFOE}}$ setup before $\overline{\text{IOW}}$ (8-bit)		230			ns
t14b	$\overline{\text{DBUFOE}}$ setup before $\overline{\text{IOW}}$ (16-bit)		165			ns
t15	$\overline{\text{DBUFOE}}$ hold after $\overline{\text{IOW}}$		50			ns
t16	MCEH delay from $\overline{\text{IOIS16}}$ active				50	ns
t17	$\overline{\text{IOW}}$ inactive from $\overline{\text{WAIT\_AB}}$ inactive		100			ns

Notes:
These timings are based on default device settings and required initial programming. These timings may be modified via the device wait state control and command delay registers. (See the Élan Am386SC300 Programmer's Reference Manual*).*

1. *$\overline{\text{WAIT\_AB}}$ asserted for greater than 10 µs may cause a DRAM $\overline{\text{RAS}}$ Low (max) to be violated if this "extended" PCMCIA cycle occurs during a DRAM page hit. (See the t_{RASC} max parameter for a particular DRAM.) The RAS active timer (10 µs) will not force $\overline{\text{RAS}}$ inactive while the "extended" PCMCIA cycle is occurring.*

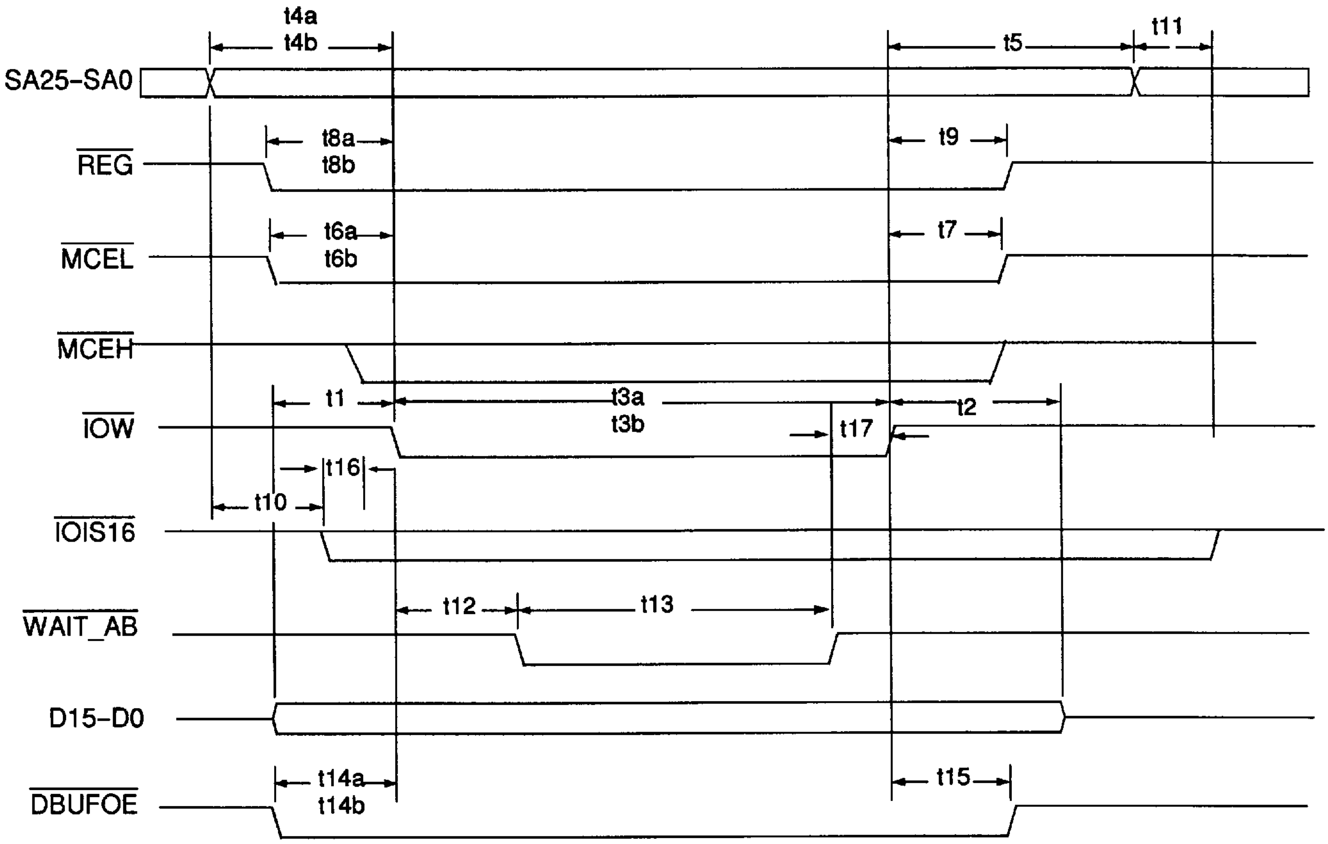


Figure 44. PCMCIA I/O Write Cycle

Table 45. Power Management Control Signals

No.	Parameter Description	Notes	Preliminary			Units
			Min	Typ	Max	
	EXTSMI pulse width		10			ns
	$\overline{\text{SUS/RES}}$ pulse width		100			ns
	$\overline{\text{LVDD}}$ active Low to $\overline{\text{LVEE}}$ active Low	1, 3				
	$\overline{\text{LVEE}}$ inactive to $\overline{\text{LVDD}}$ inactive	2, 3				

Notes:

1. *These timings are always controlled via refresh cycle generation and are therefore based on the programmed refresh rate for the system. $\overline{\text{LVEE}}$ active always follows $\overline{\text{LVDD}}$ active by one refresh cycle. This sequence will always occur when the system exits reset or when the system transitions from the Suspend mode to High Speed PLL mode. The default refresh rate after reset is 15.0 µs. See the* Élan Am386SC300 Programmer's Reference Manual *for a full description of the Power Management Unit and the refresh control mechanisms.*
2. *$\overline{\text{LVEE}}$ will always be forced to inactive whenever the device enters the Sleep mode, or whenever the Video PLL is forced off in Doze mode. $\overline{\text{LVEE}}$ will remain inactive in Suspend mode. $\overline{\text{LVDD}}$ will remain active until the device enters the Suspend mode at which point it will be forced inactive.*
3. *The LCD panel data and control signals are all forced to a logical 0 in the power management modes that are programmed to disable the video PLL (i.e., the Video PLL may be disabled in Doze, Sleep, and Suspend modes.) These signals will be re-driven whenever $\overline{\text{LVDD}}$ is driven active.*

Table 46. BIOS ROM Read/Write 8-Bit Cycle

Symbol	Parameter Description	Notes	Preliminary Min	Preliminary Typ	Preliminary Max	Units
t1a	SA stable to $\overline{\text{ROMCS}}$ active	1			55	ns
t1b	SA stable to $\overline{\text{ROMCS}}$ active	2			5	ns
t2a	SA hold from $\overline{\text{ROMCS}}$ inactive Write	1	50			ns
t2b	SA hold from $\overline{\text{ROMCS}}$ inactive Read	1	0			ns
t3a	$\overline{\text{ROMCS}}$ pulse width Read	1	390			ns
t3b	$\overline{\text{ROMCS}}$ pulse width Write	1	335			ns
t4a	$\overline{\text{MEMW}}$ active to $\overline{\text{ROMCS}}$ active	1			2	ns
t4b	$\overline{\text{MEMR}}$ active to $\overline{\text{ROMCS}}$ active	1			1	ns
t5a	$\overline{\text{ROMCS}}$ hold from $\overline{\text{MEMW}}$ inactive	1	0			ns
t5b	$\overline{\text{ROMCS}}$ hold from $\overline{\text{MEMR}}$ inactive	1	0			ns
t6	RDDATA setup to command inactive		40			ns
t7	RDDATA hold from command inactive		0			ns
t8	WRDATA setup to command inactive		200			ns
t9	WRDATA hold from command inactive		50			ns
t10	$\overline{\text{DBUFOE}}$ active from command				5	ns
t11a	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMW}}$		50			ns
t11b	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMR}}$		–2			ns
t12	ENDIRH, ENDIRL setup before $\overline{\text{MEMR}}$				50	ns
t13	ENDIRH, ENDIRL hold from $\overline{\text{MEMR}}$		–4			ns
t14	$\overline{\text{ROMCS}}$ active to command active	2			65	ns
t15	$\overline{\text{ROMCS}}$ hold from SA	2	5			ns

Notes:
These timings are based on default settings and required initial programming. These timings may be modified via the MMS Memory Wait State Select Register 1 , Index 62H,and the Command Delay Register, Index 60H. (See the Élan Am386SC300 Programmer's Reference Manual.*)*

1. *This is the timing when $\overline{\text{ROMCS}}$ is qualified with $\overline{\text{MEMR}}$ or $\overline{\text{MEMW}}$, (Bit 2 of Status Readback Register, Index B3H, = 0.)*
2. *This is the timing when $\overline{\text{ROMCS}}$ is configured as an address decode, (Bit 2 of Status Readback Register, Index B3H, = 1.)*

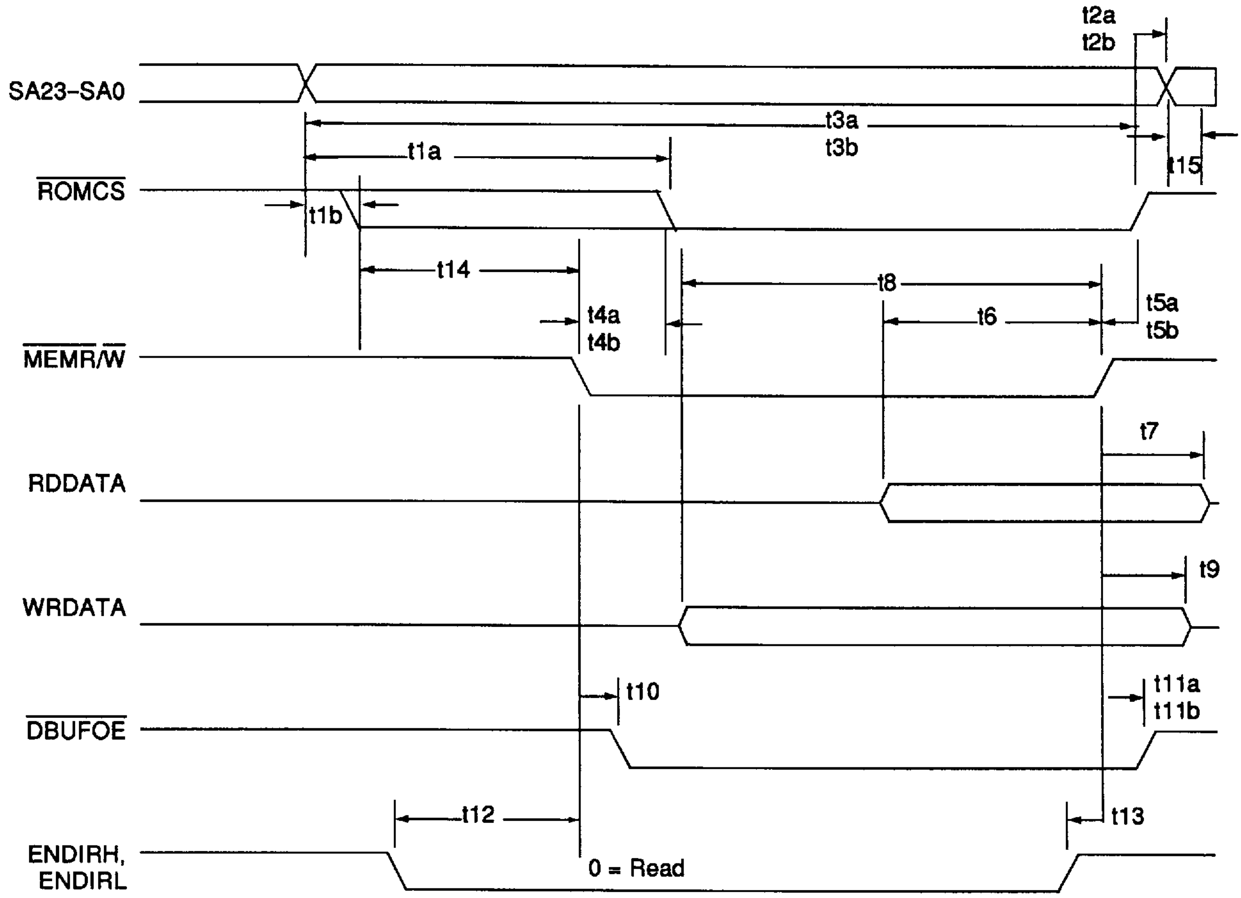


Figure 45. BIOS ROM Read/Write 8-Bit Cycle

Table 47. DOS ROM Read/Write 8-Bit Cycle

Symbol	Parameter Description	Notes	Preliminary Min	Preliminary Typ	Preliminary Max	Units
t1a	SA stable to $\overline{DOSCS}$ active	1			160	ns
t1b	SA stable to $\overline{DOSCS}$ active	2			5	ns
t2a	SA hold from $\overline{DOSCS}$ inactive Write	1	50			ns
t2b	SA hold from $\overline{DOSCS}$ inactive Read	1	0			ns
t3a	$\overline{DOSCS}$ pulse width Read	1	550			ns
t3b	$\overline{DOSCS}$ pulse width Write	1	500			ns
t4a	$\overline{MEMW}$ active to $\overline{DOSCS}$ active	1			4	ns
t4b	$\overline{MEMR}$ active to $\overline{DOSCS}$ active	1			4	ns
t5a	$\overline{DOSCS}$ hold from $\overline{MEMW}$ inactive	1			0	ns
t5b	$\overline{DOSCS}$ hold from $\overline{MEMR}$ inactive	1			0	ns
t6	RDDATA setup to command inactive		40			ns
t7	RDDATA hold from command inactive		0			ns
t8	WRDATA setup to command inactive		90			ns
t9	WRDATA hold from command inactive		50			ns
t10	$\overline{DBUFOE}$ active from command				5	ns
t11a	$\overline{DBUFOE}$ hold from $\overline{MEMW}$		50			ns
t11b	$\overline{DBUFOE}$ hold from $\overline{MEMR}$		-2			ns
t12	ENDIRH, ENDIRL setup to $\overline{MEMR}$				50	ns
t13	ENDIRH, ENDIRL hold from $\overline{MEMR}$		-3			ns
t14	$\overline{DOSCS}$ active to command active	2			170	ns
t15	$\overline{DOSCS}$ hold from SA	2	5			ns

Notes:

These timings are based on default settings and required initial programming. These timings may be modified via the MMS Memory Wait State Select Register 1 , Index 62H, and the Command Delay Register, Index 60H. (See the Élan Am386SC300 Programmer's Reference Manual.*)*

1. *This is the timing when $\overline{DOSCS}$ is qualified with $\overline{MEMR}$ or $\overline{MEMW}$, (Bit 4 of ROM Configuration Register 3, Index B8H, = 0).*
2. *This is the timing when $\overline{DOSCS}$ is configured as an address decode, (Bit 4 of ROM Configuration Register 3, Index B8H, = 1).*

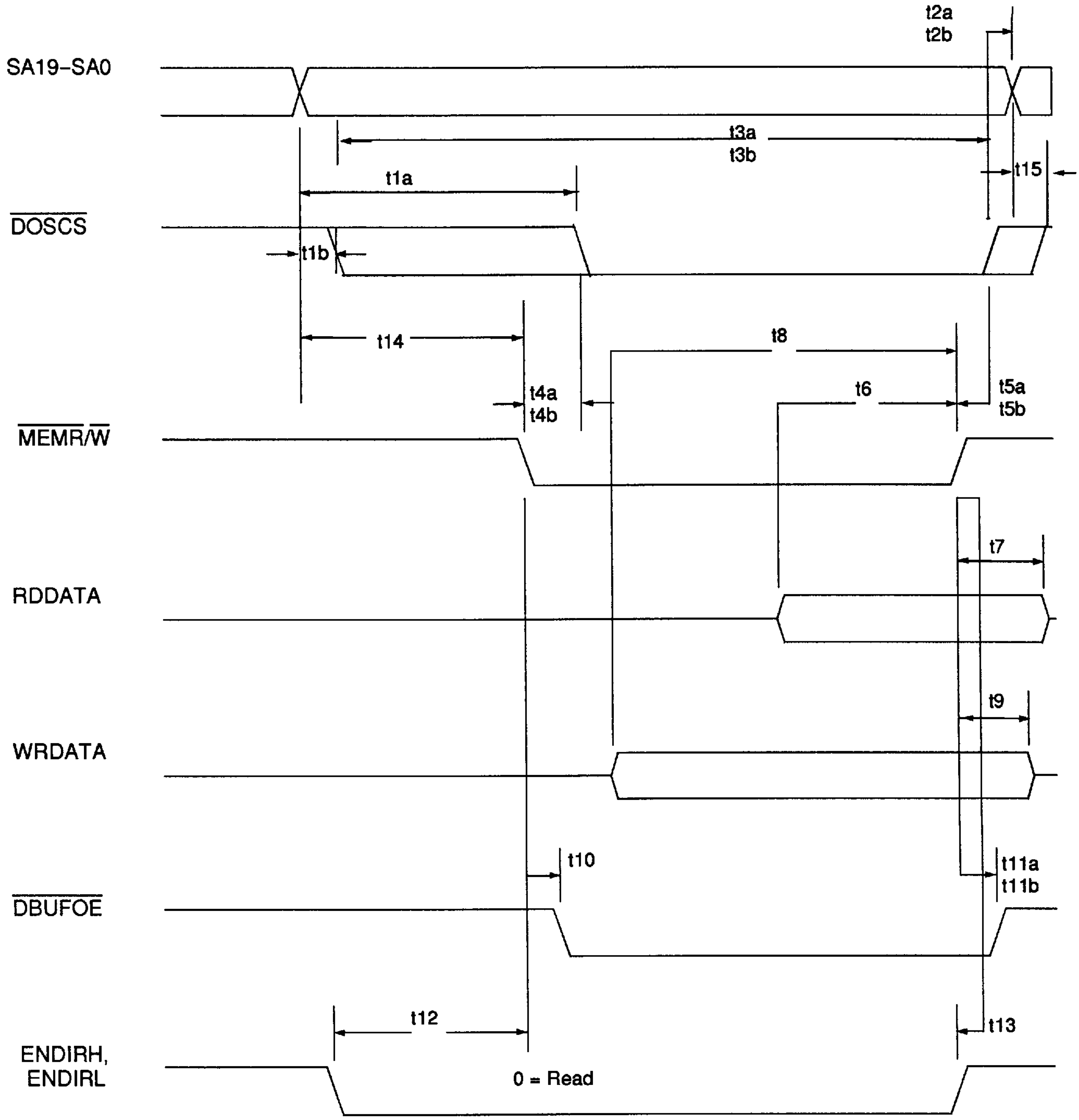


Figure 46. DOS ROM Read/Write 8-Bit Cycle

Table 48. DOS ROM Read/Write 16-Bit Cycle (See Figure 47)

Symbol	Parameter Description	Notes	Preliminary Min	Preliminary Typ	Preliminary Max	Units
t1a	SA stable to $\overline{\text{DOSCS}}$ active	1			65	ns
t1b	SA stable to $\overline{\text{DOSCS}}$ active	2			5	ns
t2a	SA hold from $\overline{\text{DOSCS}}$ inactive Write	1	50			ns
t2b	SA hold from $\overline{\text{DOSCS}}$ inactive Read	1	0			ns
t3a	$\overline{\text{DOSCS}}$ pulse width Read	1	550			ns
t3b	$\overline{\text{DOSCS}}$ pulse width Write	1	500			ns
t4a	$\overline{\text{MEMW}}$ active to $\overline{\text{DOSCS}}$	1			3	ns
t4b	$\overline{\text{MEMR}}$ active to $\overline{\text{DOSCS}}$ active	1			4	ns
t5a	$\overline{\text{DOSCS}}$ hold from $\overline{\text{MEMW}}$ inactive	1			0	ns
t5b	$\overline{\text{DOSCS}}$ hold from $\overline{\text{MEMR}}$ inactive	1			0	ns
t6	RDDATA setup to command inactive		25			ns
t7	RDDATA hold from command inactive		0			ns
t8	WRDATA setup to command inactive		400			ns
t9	WRDATA hold from command inactive		45			ns
t10	$\overline{\text{DBUFOE}}$ active from command				5	ns
t11a	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMW}}$		50			ns
t11b	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMR}}$		-2			ns
t12	ENDIRH, ENDIRL setup to $\overline{\text{MEMR}}$				50	ns
t13	ENDIRH, ENDIRL hold from $\overline{\text{MEMR}}$		−4			ns
t14	$\overline{\text{DOSCS}}$ active to command active	2			65	ns
t15	$\overline{\text{DOSCS}}$ hold from SA	2	5			ns

Note:

These timings are based on default settings and required initial programming. These timings may be modified via the MMS Memory Wait State Select Register 1 , Index 62H,and the Command Delay Register, Index 60H. (See the Élan Am386SC300 Programmer's Reference Manual.*) Bit 1 of the ROM Configuration Register 2, Index 51H, should be set for 16-bit $\overline{\text{DOSCS}}$ cycles.*

1. *This is the timing when $\overline{\text{DOSCS}}$ is qualified with $\overline{\text{MEMR}}$ or $\overline{\text{MEMW}}$, (Bit 4 of ROM Configuration Register 3, Index B8H, = 0).*
2. *This is the timing when $\overline{\text{DOSCS}}$ is configured as an address decode, (Bit 4 of ROM Configuration Register 3, Index B8H, = 1).*

Table 49. Fast DOS ROM Read/Write 16-Bit Cycle (See Figure 47)

Symbol	Parameter Description	Notes	Preliminary			Units
			Min	Typ	Max	
t1a	SA stable to $\overline{\text{DOSCS}}$ active	1			25	ns
t1b	SA stable to $\overline{\text{DOSCS}}$ active	2			5	ns
t2a	SA hold from $\overline{\text{DOSCS}}$ inactive Write	1	15			ns
t2b	SA hold from $\overline{\text{DOSCS}}$ inactive Read	1	0			ns
t3a	$\overline{\text{DOSCS}}$ pulse width Read	1	130			ns
t3b	$\overline{\text{DOSCS}}$ pulse width Write	1	145			ns
t4a	$\overline{\text{MEMW}}$ active to $\overline{\text{DOSCS}}$	1			3	ns
t4b	$\overline{\text{MEMR}}$ active to $\overline{\text{DOSCS}}$ active	1			4	ns
t5a	$\overline{\text{DOSCS}}$ hold from $\overline{\text{MEMW}}$ inactive	1			0	ns
t5b	$\overline{\text{DOSCS}}$ hold from $\overline{\text{MEMR}}$ inactive	1			0	ns
t6	RDDATA setup to command inactive		25			ns
t7	RDDATA hold from command inactive		0			ns
t8	WRDATA setup to command inactive		120			ns
t9	WRDATA hold from command inactive		15			ns
t10	$\overline{\text{DBUFOE}}$ active from command				5	ns
t11a	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMW}}$		15			ns
t11b	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMR}}$		–2			ns
t12	ENDIRH, ENDIRL setup to $\overline{\text{MEMR}}$				15	ns
t13	ENDIRH, ENDIRL hold from $\overline{\text{MEMR}}$		–4			ns
t14	$\overline{\text{DOSCS}}$ active to command active	2			15	ns
t15	$\overline{\text{DOSCS}}$ hold from $\overline{\text{SA}}$	2	5			ns

Notes:

These timings are based on default settings and required initial programming. These timings may be modified via the MMS Memory Wait State Select Register 1 , Index 62H,and the Command Delay Register, Index 60H. (See the Élan Am396SC300 Programmer's Reference Manual.*) Bit 1 of the ROM Configuration Register 2, Index 51H, should be set for 16-bit $\overline{\text{DOSCS}}$ cycles.*

1. *This is the timing when $\overline{\text{DOSCS}}$ is qualified with $\overline{\text{MEMR}}$ or $\overline{\text{MEMW}}$, (Bit 4 of ROM Configuration Register 3, Index B8H, = 0).*
2. *This is the timing when $\overline{\text{DOSCS}}$ is configured as an address decode, (Bit 4 of ROM Configuration Register 3, Index B8H, = 1).*

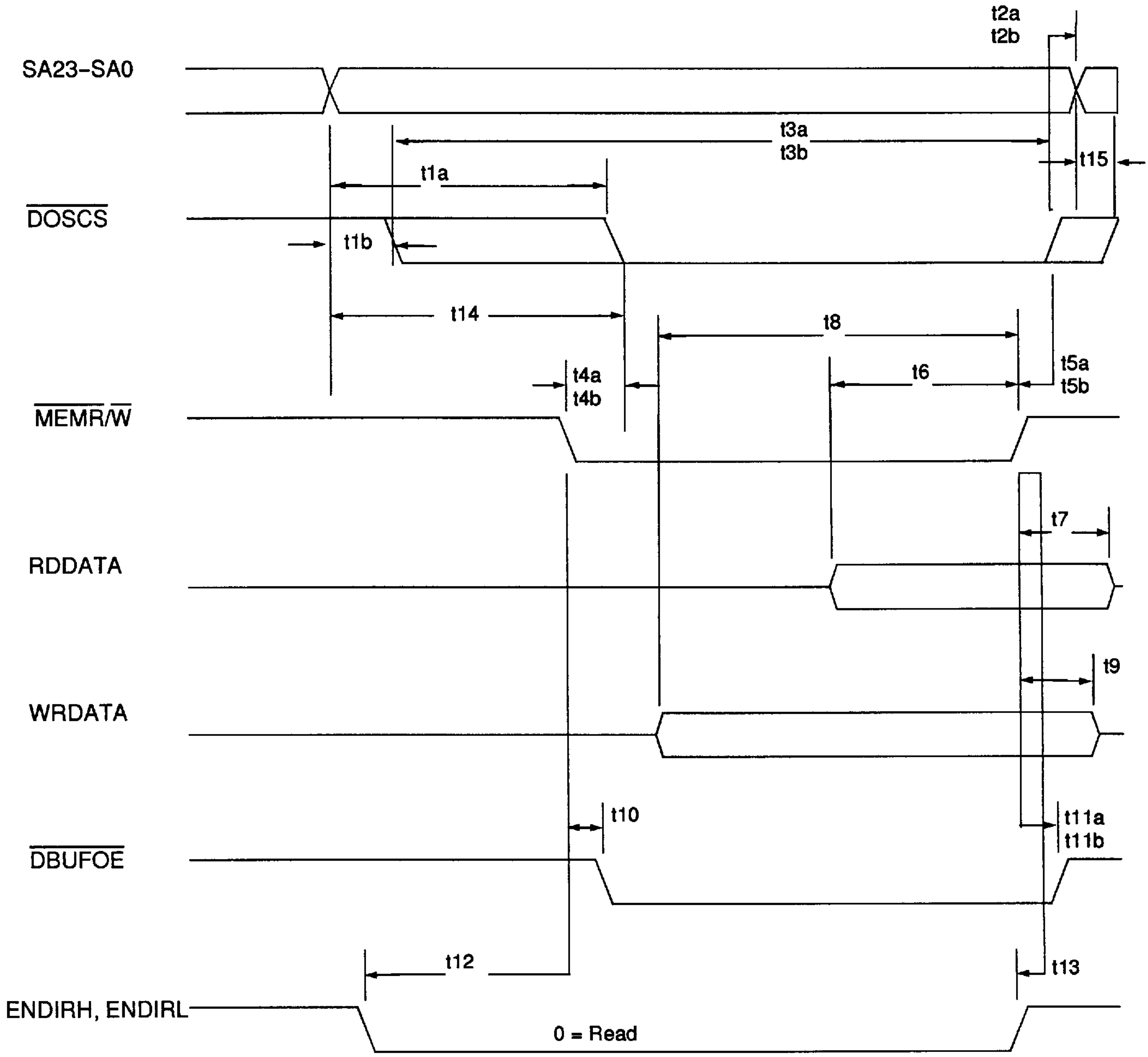


Figure 47. DOS ROM Read/Write 16-Bit Cycle

Table 50. ISA Memory Read/Write 8-Bit Cycle

Symbol	Parameter Description	Notes	Preliminary Min	Preliminary Typ	Preliminary Max	Units
t1	LA stable to BALE inactive				60	ns
t2	SA stable to command active	1			160	ns
t3	BALE pulse width		35			ns
t4	LA hold from BALE inactive		40			ns
t5a	SA hold from command inactive Write		50			ns
t5b	SA hold from command inactive Read		0			ns
t6	BALE inactive to command active				140	ns
t7a	$\overline{\text{MEMW}}$ command pulse width	1	500			ns
t7b	$\overline{\text{MEMR}}$ command pulse width	1	550			ns
t8a	$\overline{\text{MEMW}}$ active to IOCHRDY inactive				340	ns
t8b	$\overline{\text{MEMR}}$ active to IOCHRDY inactive				340	ns
t9a	$\overline{\text{MEMW}}$ hold from IOCHRDY active				110	ns
t9b	$\overline{\text{MEMR}}$ hold from IOCHRDY active				160	ns
t10	RDDATA setup to command inactive		40			ns
t11	RDDATA hold from command inactive		0			ns
t12	WRDATA setup to command inactive		300			ns
t13	WRDATA hold from command inactive		50			ns
t14	$\overline{\text{DBUFOE}}$ active from command				5	ns
t15a	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMW}}$		50			ns
t15b	$\overline{\text{DBUFOE}}$ hold from $\overline{\text{MEMR}}$		–2			ns
t16	ENDIRH, ENDIRL setup to $\overline{\text{MEMR}}$		170			ns
t17	ENDIRH, ENDIRL hold from $\overline{\text{MEMR}}$		–4			ns

Note:

These timings are based on default settings and required initial programming. These timings may be modified via the MMS Memory Wait State Select Register 1, Index 62H, and the Command Delay Register, Index 60H. (See the Élan Am386SC300 Programmer's Reference Manual.*)*

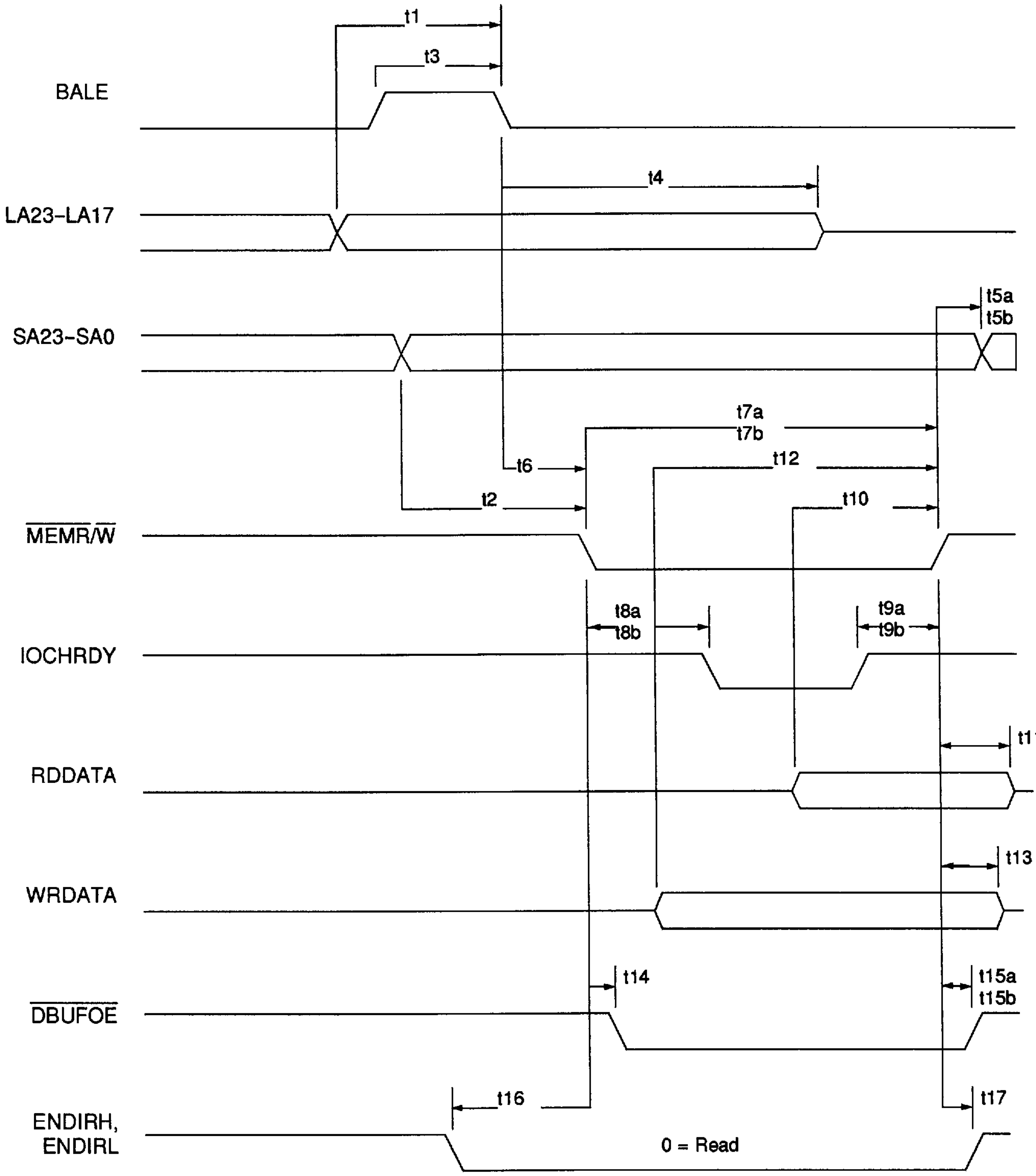


Figure 48. ISA Memory Read/Write 8-Bit Cycle

Table 51. ISA Memory Read/Write 16-Bit Cycle

Symbol	Parameter Description	Notes	Preliminary Min	Preliminary Typ	Preliminary Max	Units
t1	LA stable to BALE inactive				60	ns
t2	SA stable to command active	1			70	ns
t3	BALE pulse width		35			ns
t4	LA hold from BALE inactive		40			ns
t5a	SA hold from command inactive Write		50			ns
t5b	SA hold from command inactive Read		0			ns
t6	BALE inactive to command active				30	ns
t7a	LA stable to MCS16 valid				35	ns
t7b	MCS16 hold from LA change		0			ns
t8a	MEMW command pulse width	1	500			ns
t8b	MEMR command pulse width	1	550			ns
t9a	MEMW active to IOCHRDY inactive				340	ns
t9b	MEMR active to IOCHRDY inactive				340	ns
t10a	MEMW hold from IOCHRDY active				110	ns
t10b	MEMR hold from IOCHRDY active				160	ns
t11	RDDATA setup to command inactive		25			ns
t12	RDDATA hold from command inactive		0			ns
t13	WRDATA setup to command inactive		330			ns
t14	WRDATA hold from command inactive		50			ns
t15	DBUFOE active from command				5	ns
t16a	DBUFOE hold from command Write		50			ns
t16b	DBUFOE hold from command Read		-2			ns
t17	ENDIRH, ENDIRL setup to MEMR				50	ns
t18	ENDIRH, ENDIRL hold from MEMR		-4			ns
t19	SA (23:13) stable to MCS16 valid				25	ns

Note:
These timings are based on default settings and required initial programming. These timings may be modified via the MMS Memory Wait State Select Register 1, Index 62H, and the Command Delay Register, Index 60H. (See the Élan Am386SC300 Programmer's Reference Manual.*)*

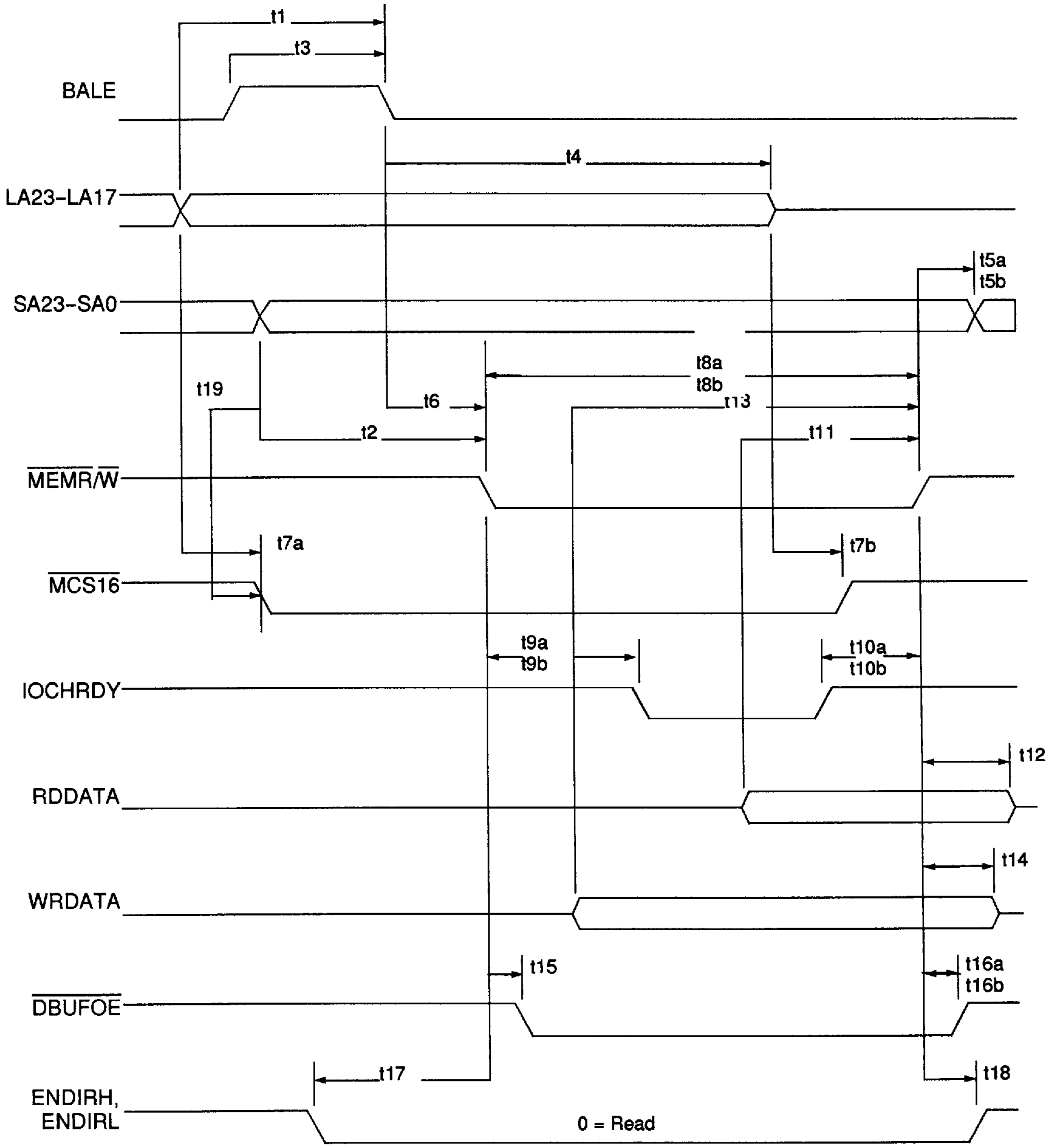


Figure 49. ISA Memory Read/Write 16-Bit Cycle

Table 52. ISA Memory Read/Write 0 Wait State Cycle

Symbol	Parameter Description	Notes	Preliminary			Units
			Min	Typ	Max	
t1	LA stable to BALE inactive				60	ns
t2	SA stable to command active				70	ns
t3	BALE pulse width		35			ns
t4	LA hold from BALE inactive		40			ns
t5a	SA hold from command inactive Write		0			ns
t5b	SA hold from command inactive Read		0			ns
t6	BALE inactive to command active				30	ns
t7	LA stable to $\overline{\text{MCS16}}$ active				35	ns
t8	Command pulse width		100			ns
t9	Command active to $\overline{\text{OWS}}$ active		0		20	ns
t10	$\overline{\text{OWS}}$ hold from command inactive				40	ns
t11	$\overline{\text{MCS16}}$ hold from LA change		0			ns
t12	RDDATA setup to command inactive		25			ns
t13	RDDATA hold from command inactive		0			ns
t14	WRDATA setup to command inactive		100			ns
t15	WRDATA hold from command inactive	1	–1			ns

Notes:
These timings are based on default settings and required initial programming. These timings may be modified via the MMS Memory Wait State Select Register 1, Index 62H, and the Command Delay Register, Index 60H. (See the Élan Am386SC300 Programmer's Reference Manual.*)*

1. *If the data bus is externally buffered and/or level translated, this write data hold time will be increased by the propagation delay through the buffer and/or the output disable delay of the buffer.*

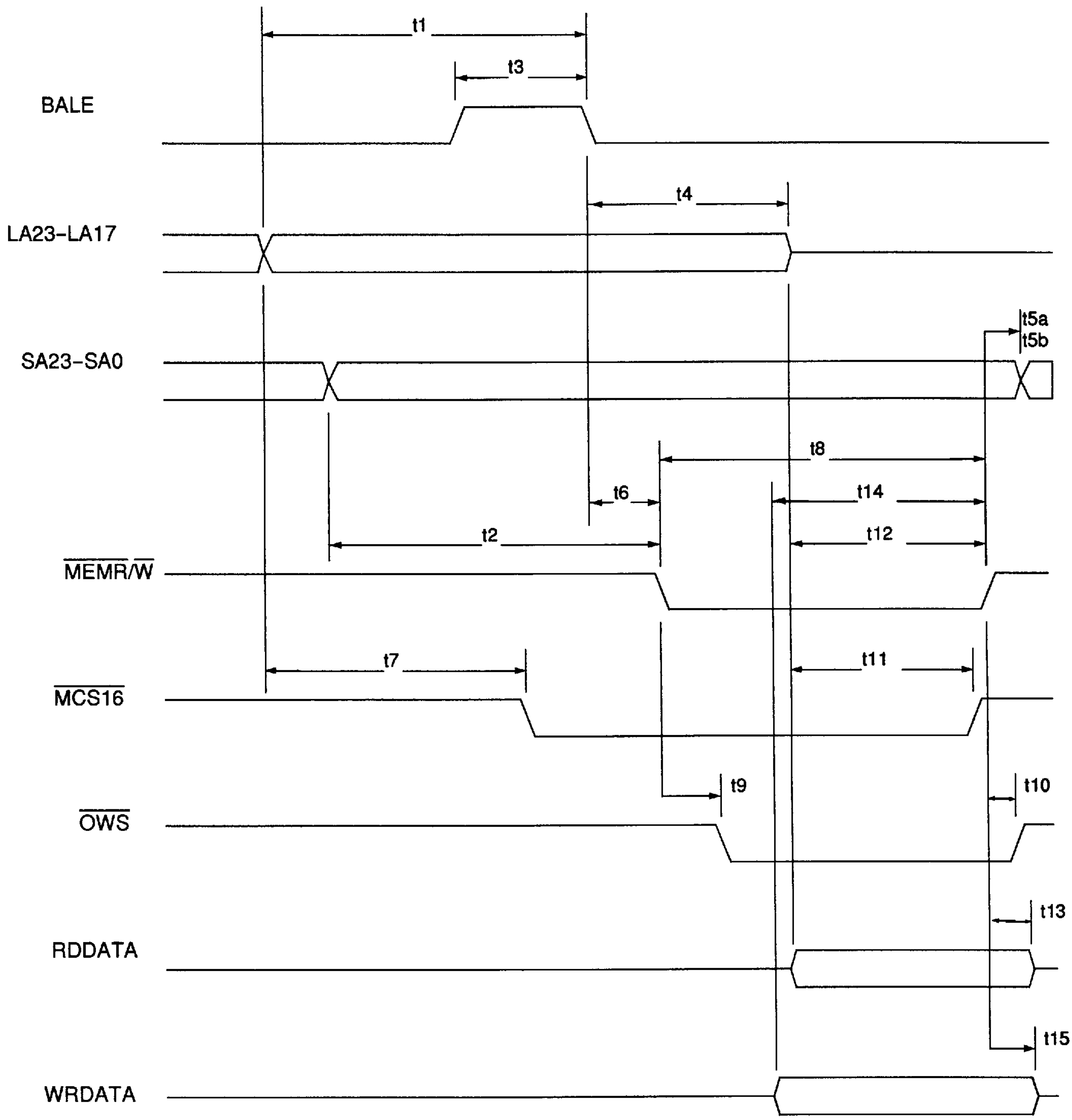


Figure 50. ISA Memory Read/Write 0 Wait State Cycle

Table 53. ISA I/O 8-Bit Read/Write Cycle

Symbol	Parameter Description	Notes	Preliminary			Units
			Min	Typ	Max	
t1a	SA stable to $\overline{\text{IOW}}$ active				200	ns
t1b	SA stable to $\overline{\text{IOR}}$ active				150	ns
t2a	SA hold from $\overline{\text{IOW}}$ inactive		50			ns
t2b	SA hold from $\overline{\text{IOR}}$ inactive		0			ns
t3a	$\overline{\text{IOW}}$ pulse width		450			ns
t3b	$\overline{\text{IOR}}$ pulse width		550			ns
t4a	$\overline{\text{IOW}}$ active to IOCHRDY inactive				300	ns
t4b	$\overline{\text{IOR}}$ active to IOCHRDY inactive				350	ns
t5a	$\overline{\text{IOW}}$ hold from IOCHRDY active		110			ns
t5b	$\overline{\text{IOR}}$ hold from IOCHRDY active		160			ns
t6	RDDATA setup to command inactive		40			ns
t7	RDDATA hold from command inactive		0			ns
t8	WRDATA setup to command inactive		400			ns
t9	WRDATA hold from command inactive		50			ns
t10	$\overline{\text{DBUFOE}}$ active from command				5	ns
t11a	$\overline{\text{DBUFOE}}$ hold from command Write		50			ns
t11b	$\overline{\text{DBUFOE}}$ hold from command Read		-2			ns
t12	ENDIRH, ENDIRL setup to $\overline{\text{IOR}}$				150	ns
t13	ENDIRH, ENDIRL hold from $\overline{\text{IOR}}$		-4			ns

Note:
These timings may be modified via the MMS Memory Wait State Select Register 1, Index 62H, and the Command Delay Register, Index 60H. (See the Élan Am386SC300 Programmer's Reference Manual.*)*

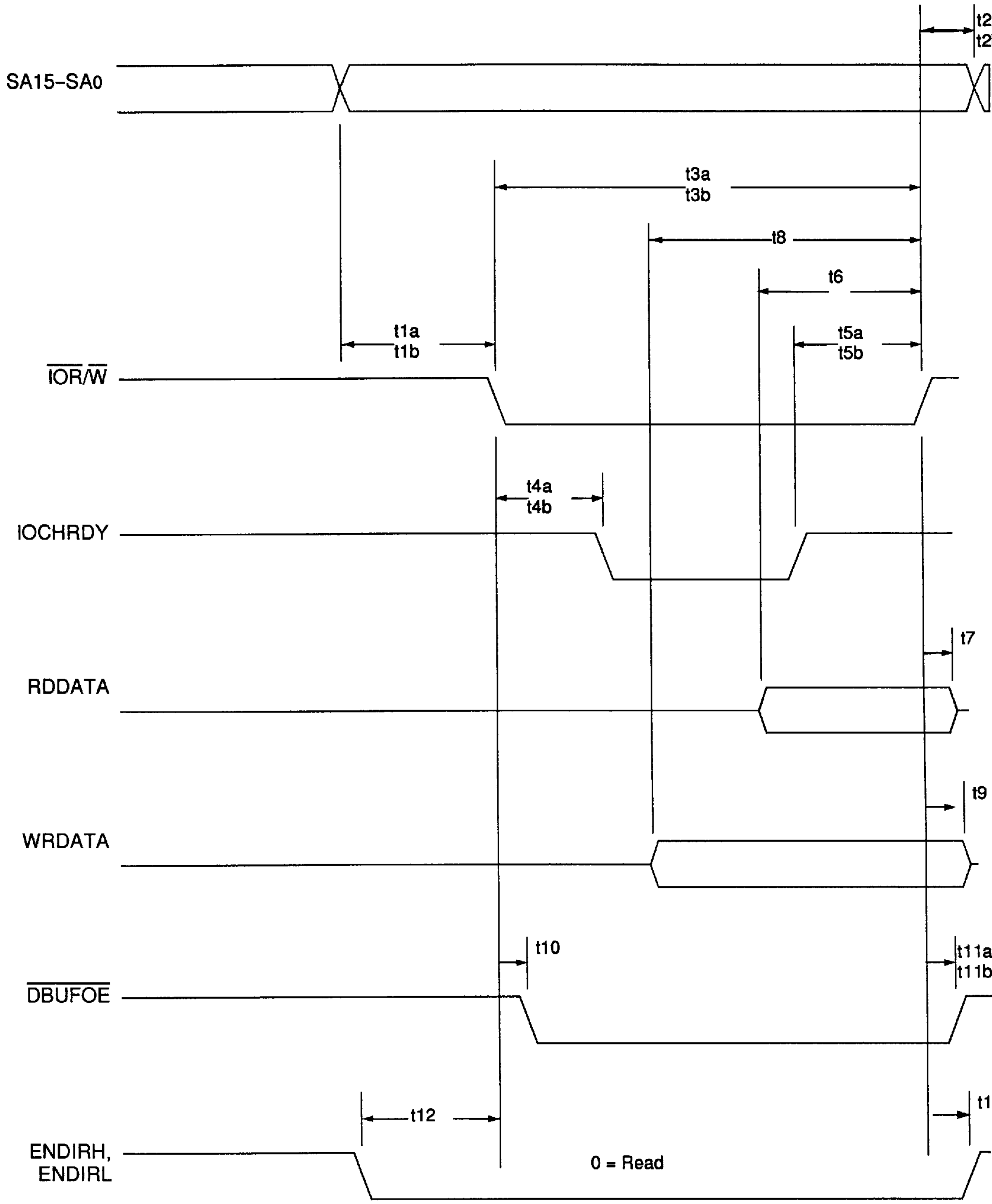


Figure 51. ISA I/O 8-Bit Read/Write Cycle

Table 54. ISA I/O 16-Bit Read/Write Cycle

Symbol	Parameter Description	Notes	Preliminary			Units
			Min	Typ	Max	
t1a	SA stable to $\overline{\text{IOW}}$ active				150	ns
t1b	SA stable to $\overline{\text{IOR}}$ active				100	ns
t2	SA stable to $\overline{\text{IOCS16}}$ active				95	ns
t3a	$\overline{\text{IOW}}$ active to IOCHRDY inactive				30	ns
t3b	$\overline{\text{IOR}}$ active to IOCHRDY inactive				80	ns
t4a	$\overline{\text{IOW}}$ hold from IOCHRDY active		110			ns
t4b	$\overline{\text{IOR}}$ hold from IOCHRDY active		160			ns
t5a	$\overline{\text{IOW}}$ pulse width		160			ns
t5b	$\overline{\text{IOR}}$ pulse width		260			ns
t6a	SA hold from $\overline{\text{IOW}}$ inactive		50			ns
t6b	SA hold from $\overline{\text{IOR}}$ inactive		0			ns
t7	RDDATA setup to command inactive		40			ns
t8	RDDATA hold from command inactive		0			ns
t9	WRDATA setup to command inactive		250			ns
t10	WRDATA hold from command inactive		50			ns
t11	$\overline{\text{DBUFOE}}$ active from command				5	ns
t12a	$\overline{\text{DBUFOE}}$ hold from command Write		50			ns
t12b	$\overline{\text{DBUFOE}}$ hold from command Read		-2			ns
t13	ENDRIH, ENDIRL setup to $\overline{\text{IOR}}$				100	ns
t14	ENDIRH, ENDIRL hold from $\overline{\text{IOR}}$		–4			ns

Note:
These timings are based on default settings and required initial programming. These timings may be modified via the MMS Memory Wait State Select Register 1, Index 62H, and the Command Delay Register, Index 60H. (See the Élan Am386SC300 Programmer's Reference Manual.*)*

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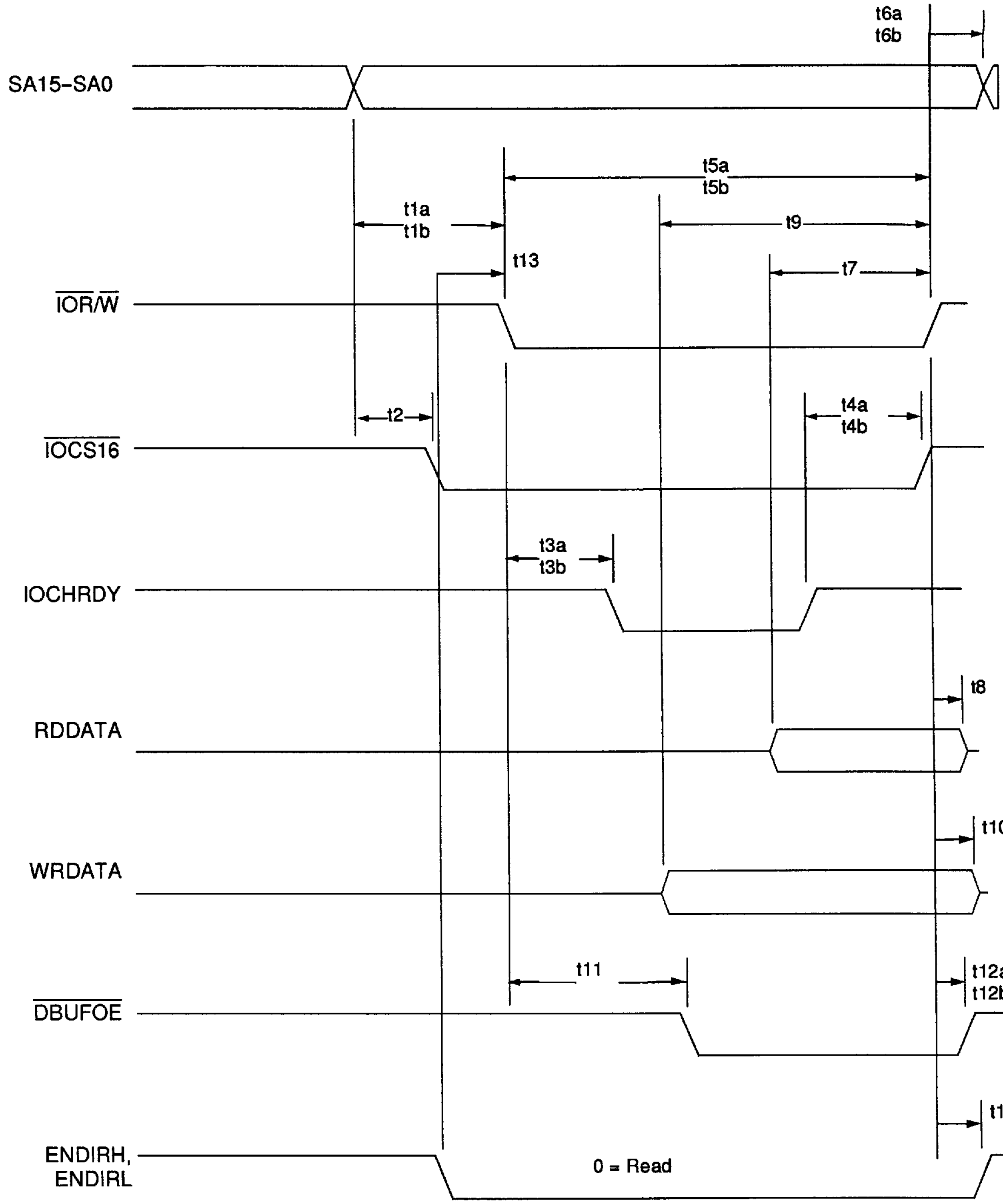

Figure 52. ISA I/O 16-Bit Read/Write Cycle

Table 55. EPP Data Register Write Cycle

Symbol	Parameter Description	Max	Min	Unit
t0	$\overline{AFDT}$ delay from $\overline{IOW}$ active	8.4	4.9	ns
t1	$\overline{AFDT}$ delay from $\overline{PPDCS}$ active	1.8	1.1	ns
t2	$\overline{AFDT}$ delay from $\overline{PPOEN}$ active	1.0	0.8	ns
t3	$\overline{AFDT}$ active pulse width (no wait states added)	450	448	ns
t4	$\overline{AFDT}$ High to Low recovery	1000		ns
t5	$\overline{AFDT}$ Low to $\overline{STRB}$ Low	−0.2		ns
t6	$\overline{STRB}$ delay from $\overline{PPDCS}$ active	1.6	0.9	ns
t7	$\overline{STRB}$ delay from $\overline{PPOEN}$ active	0.8	0.6	ns
t8	$\overline{AFDT}$ High to $\overline{STRB}$ High delay	−2.4	−1.4	ns
t9	$\overline{STRB}$ Low to data valid delay	3.7		ns
t10	$\overline{STRB}$ High to data valid hold		4.0	ns
t11	$\overline{PPOEN}$ delay from $\overline{IOW}$ active	7.4		ns
t12	$\overline{PPOEN}$ delay from $\overline{IOW}$ inactive		1.1	ns
t13	$\overline{PPDCS}$ delay from $\overline{IOW}$ active	6.6		ns
t14	$\overline{PPDCS}$ delay from $\overline{IOW}$ inactive		4.3	ns
t15	$\overline{AFDT}$ hold from BUSY High	139	129	ns
t16	BUSY Low delay from $\overline{AFDT}$ active	307		ns

Notes:
The appropriate timings above are valid for the Bidirectional Parallel Port mode also. Timings t13 and t14 are also valid for the Unidirectional Parallel Port mode. (PPDCS is PPWDE in Unidirectional mode.)

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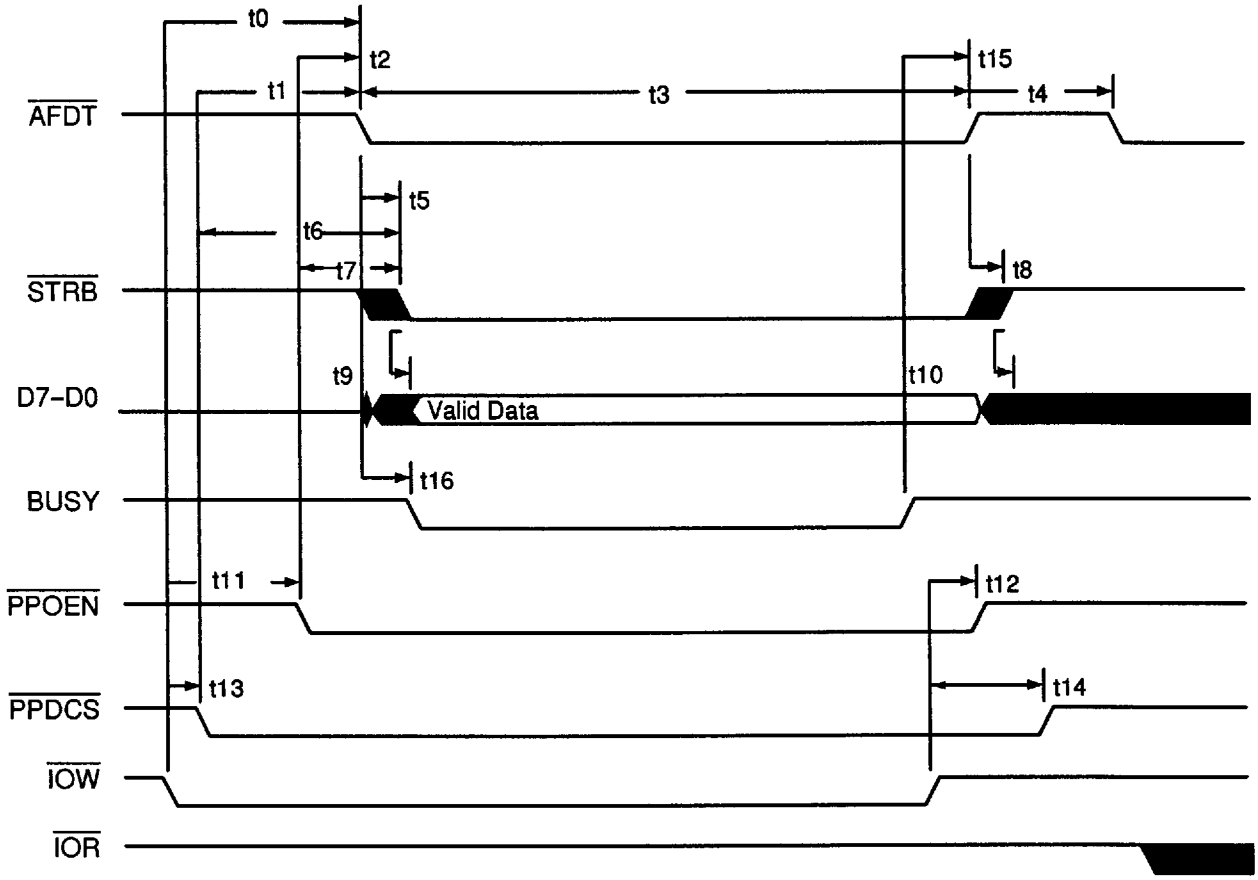


Figure 53. EPP Data Register Write Cycle

Table 56. EPP Data Register Read Cycle

Symbol	Parameter Description	Max	Min	Unit
t1	$\overline{\text{AFDT}}$ delay from $\overline{\text{PPDCS}}$ active	1.8	1.1	ns
t2	$\overline{\text{AFDT}}$ active pulse width (no wait states)	450	448	ns
t3	$\overline{\text{AFDT}}$ High to Low recovery	1000		ns
t4	Read data valid delay	25.3		ns
t5	Read data hold time		2.3	ns
t6	$\overline{\text{PPDCS}}$ delay from $\overline{\text{IOR}}$ active	6.8		ns
t7	$\overline{\text{PPDCS}}$ delay from $\overline{\text{AFDT}}$ inactive	3.7	1.8	ns
t8	$\overline{\text{PPDCS}}$ delay from $\overline{\text{IOR}}$ inactive		4.2	ns
t9	BUSY (inactive) hold from $\overline{\text{AFDT}}$ High		0	ns

Note:
The appropriate timings above are also valid for the Bidirectional Parallel Port mode.

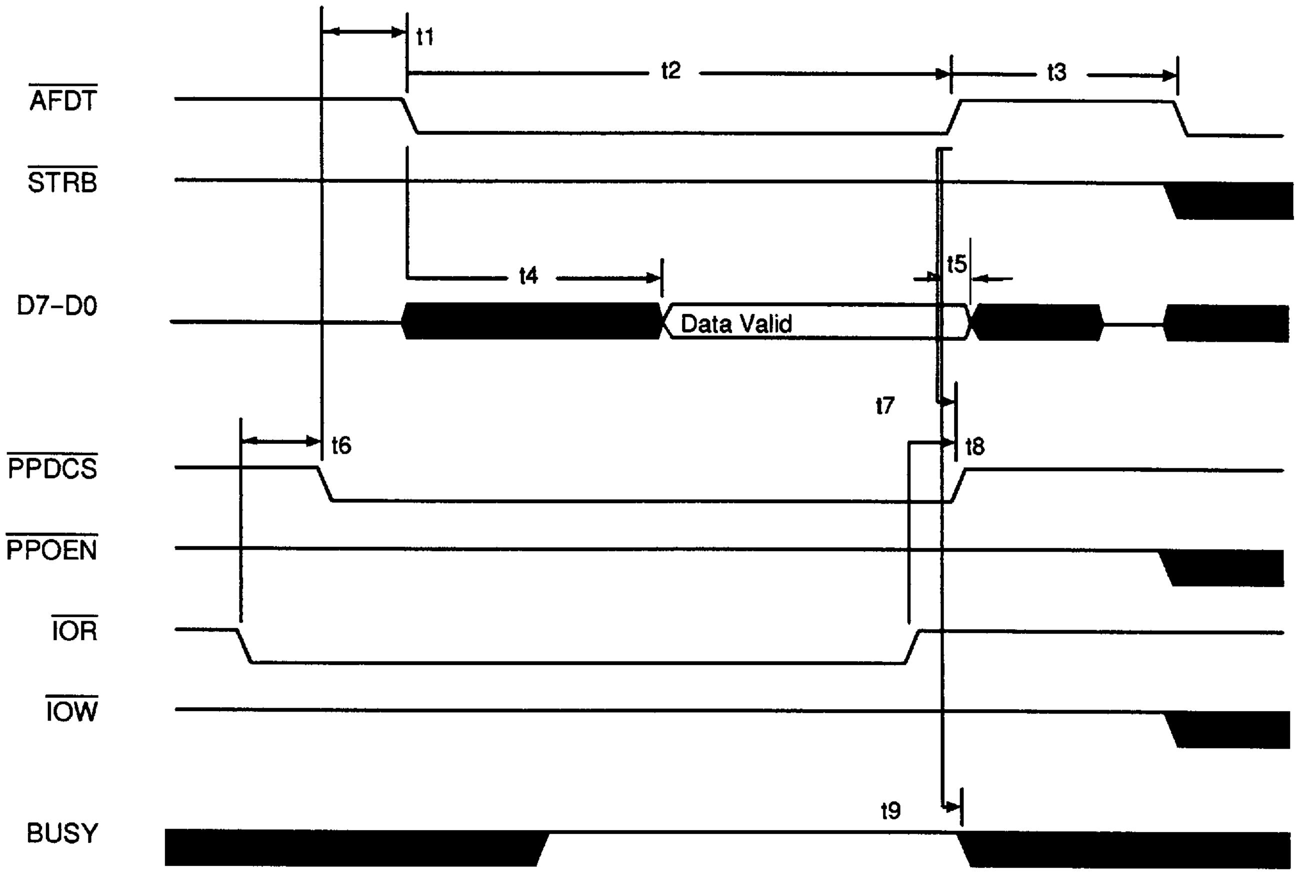
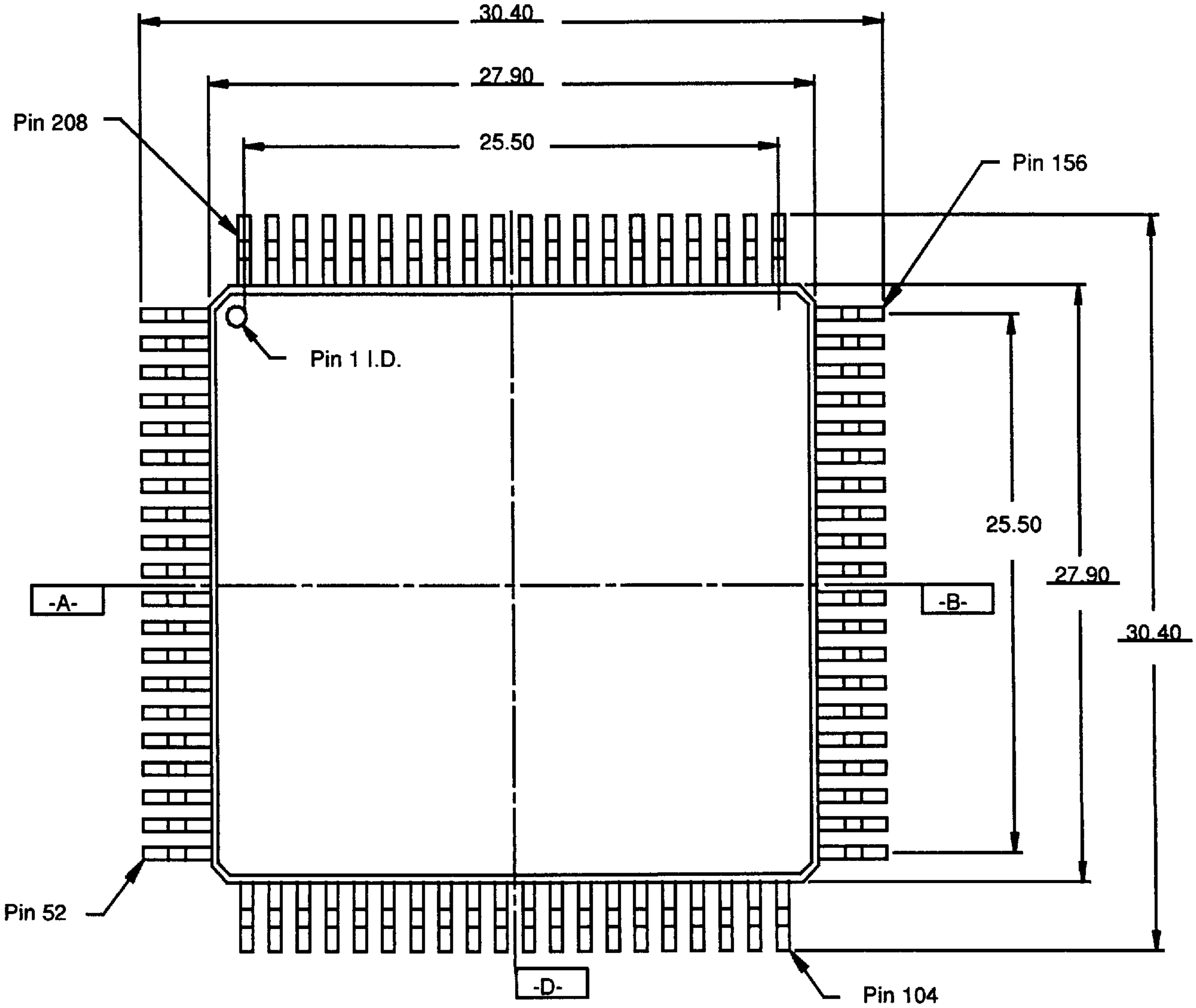
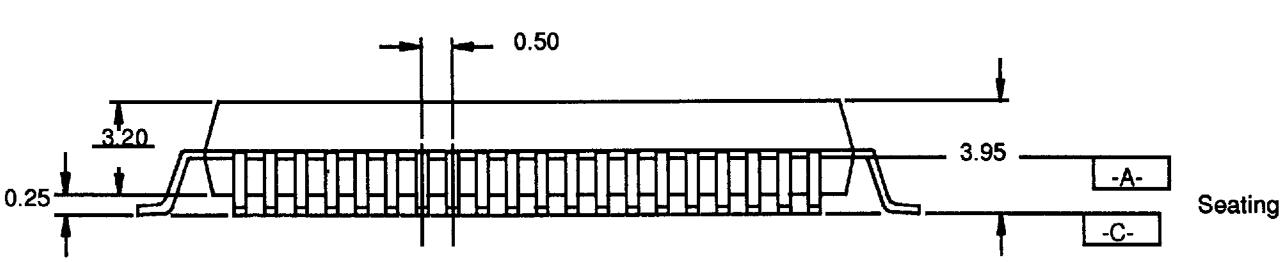


Figure 54. EPP Data Register Read Cycle

PHYSICAL DIMENSIONS
PQR 208, Trimmed and Formed
Plastic Quad Flat Pack



Top View



Side View

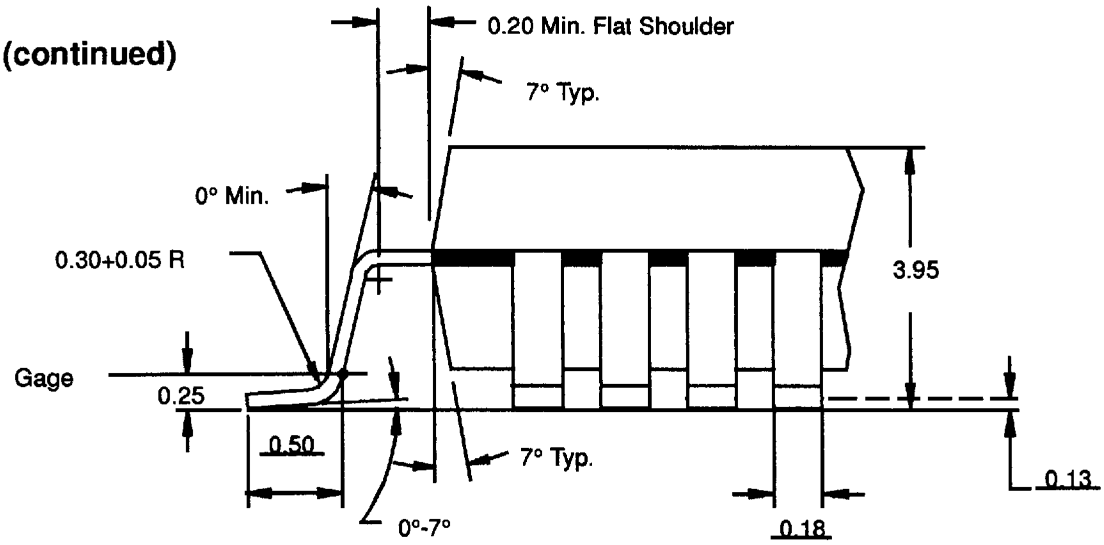
Notes:

8. All measurements are in millimeters unless otherwise noted.

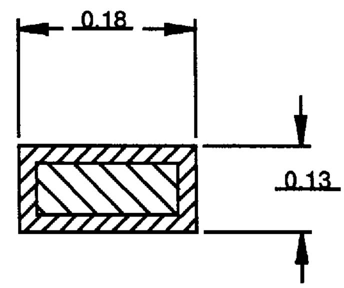
2. Not to scale. For reference only.

pqr208

PQR 208 (continued)



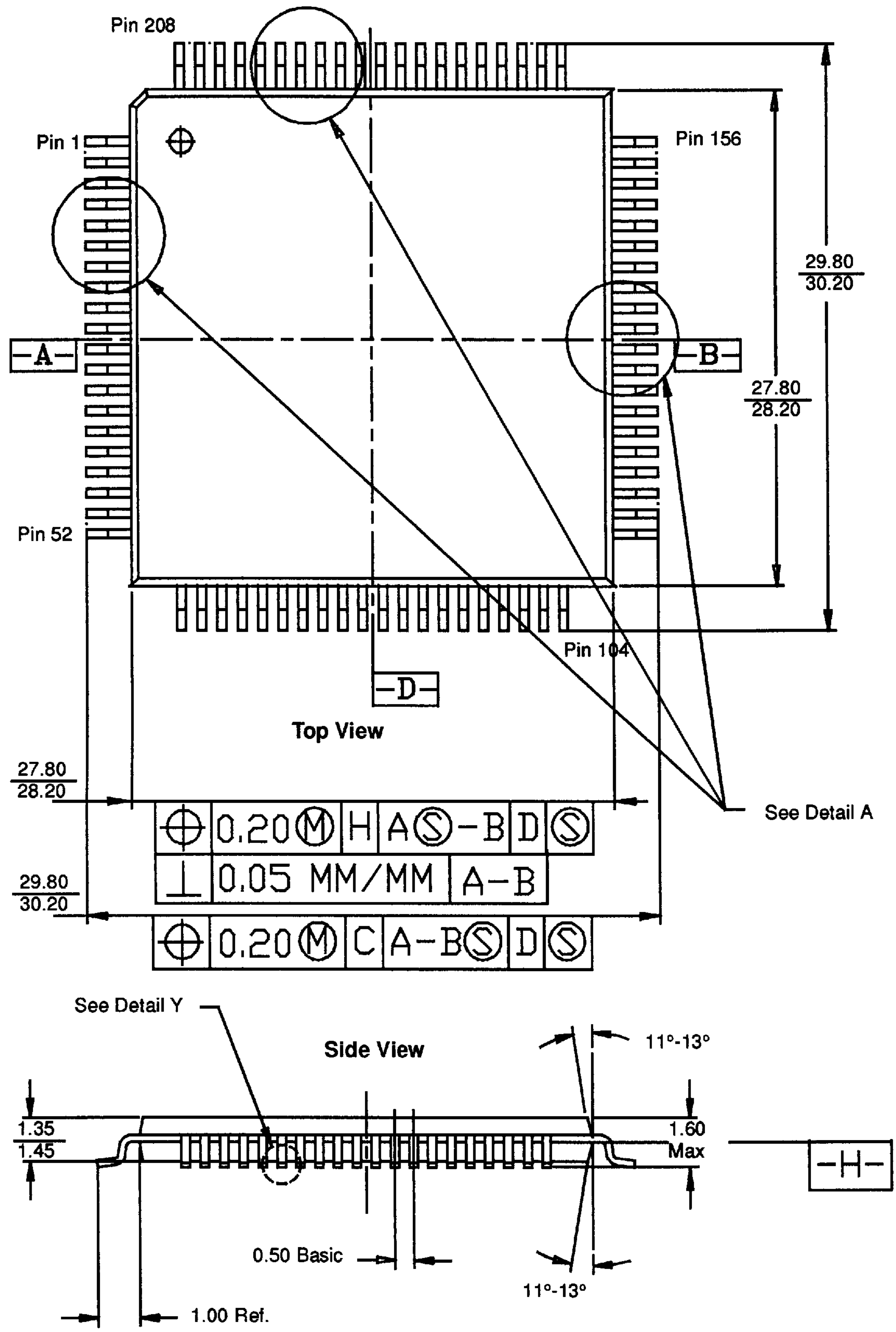
Detail X

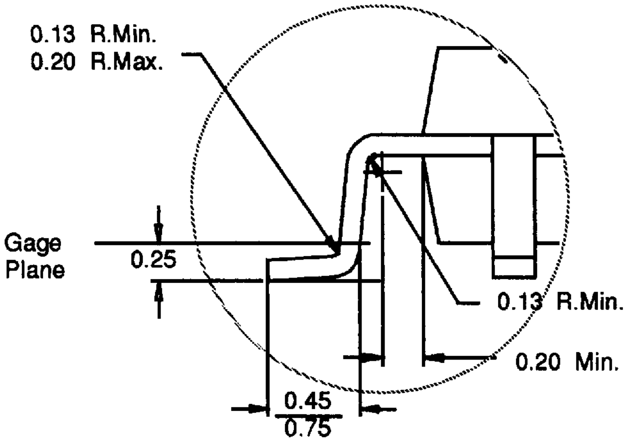


Section S-S

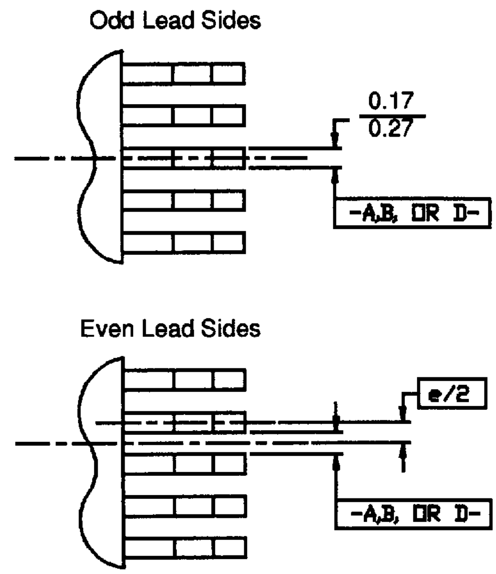
Notes:

PHYSICAL DIMENSIONS
PQR 208, Trimmed and Formed
Thin Quad Flat Pack

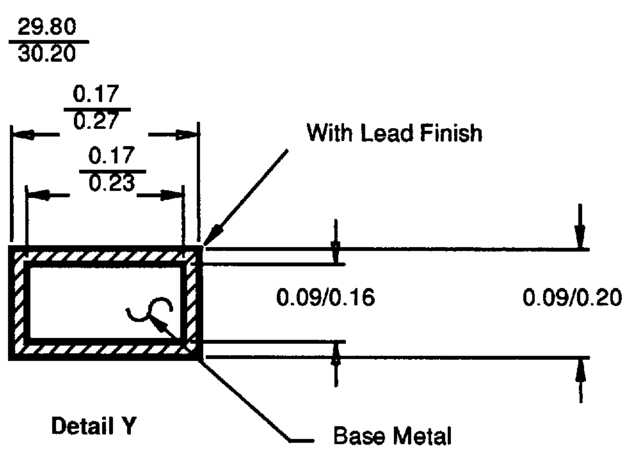




Detail X



See Detail A



Detail Y